

# Loveland Schematics

## Skylake-U

2015-09-18

REV : A00

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*DY : None Installed*

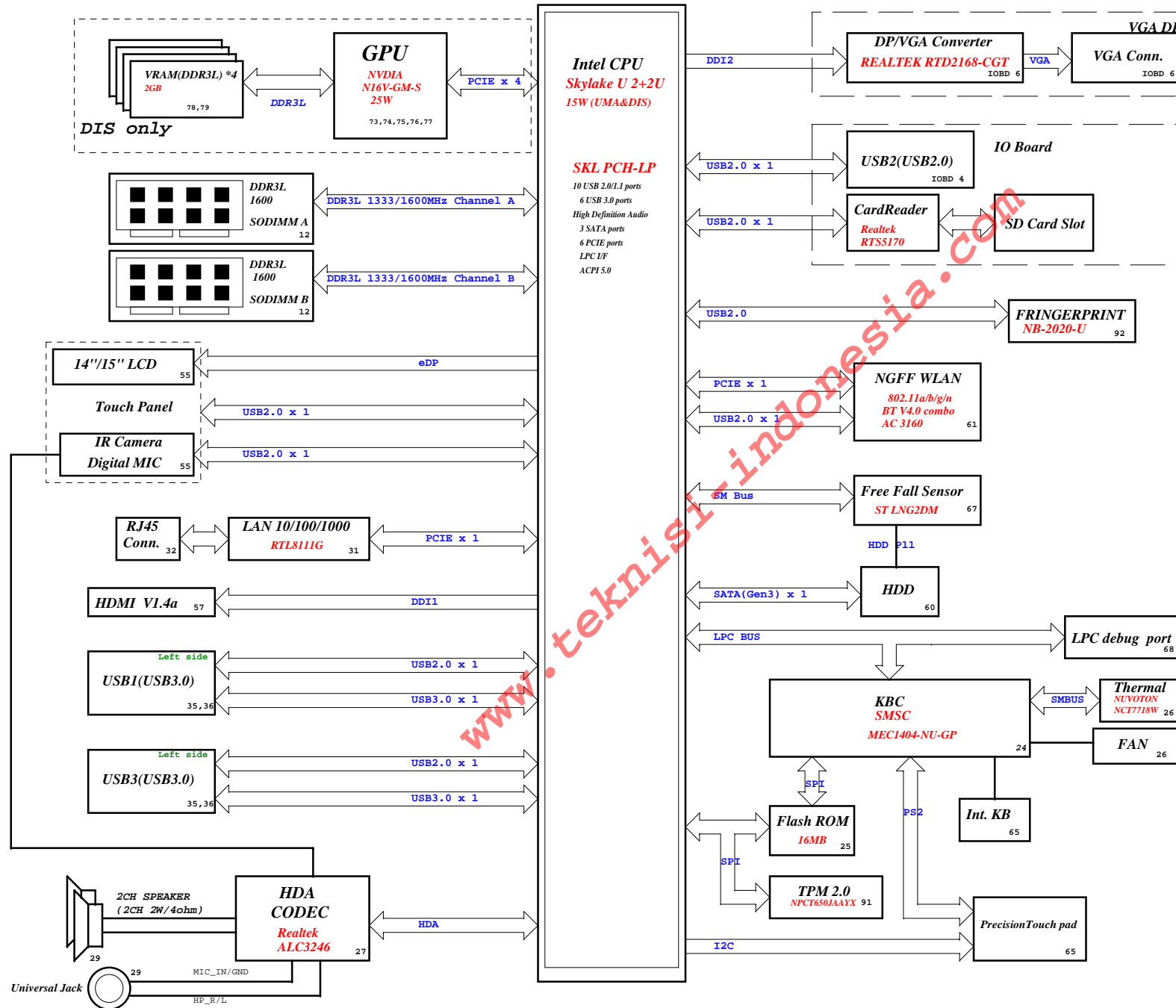
*UMA: UMA only installed*

*OPS: DISCRTE OPTIMUS installed*

<Variant Name>		
<b>DELL</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>Cover Page</b>		
Size A3	Document Number <b>Loveland SKL-U</b>	Rev <b>A00</b>
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Project code:  
Love14 SKL --> 4PD060010001  
Love15 SKL --> 4PD061010001  
PCB P/N: 14291  
Revision: A00

## Loveland SKL-U Block Diagram



CHARGER	
BQ24780RUYR 44	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	DCBATOUT
SYSTEM DC/DC	
RT6576DGQW 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5
CPU Core Power	
NCP81208MNTXG 46-50 NCP81382MNTXG X2 NCP81253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE +VCCGT +VCCSA
DDR3L SUS	
TPS51716RUKR 51	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0
CPU DCDC-V1D00A	
SY8208DQNC 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
LDO-V1D5V	
S-1339D15-M5001 54	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
LDO-V1D8V	
APL5930KAI-TRG 54	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
5V/3V_S0	
G5016KD1U 40	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0
VCCSTG	
M5938ARD1U 40	
INPUTS	OUTPUTS
5V_S5	+VCCIO +VCCSTG
VCCST	
M5938ARD1U 40	
INPUTS	OUTPUTS
5V_S5	+V1.00U_CPU +VCCSTP_CPU
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Bottom	

<Core Design>

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Title: **Block Diagram**

Size: A2 Document Number: **Loveland SKL-U** Rev: <RevCode>


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Main Func = CPU

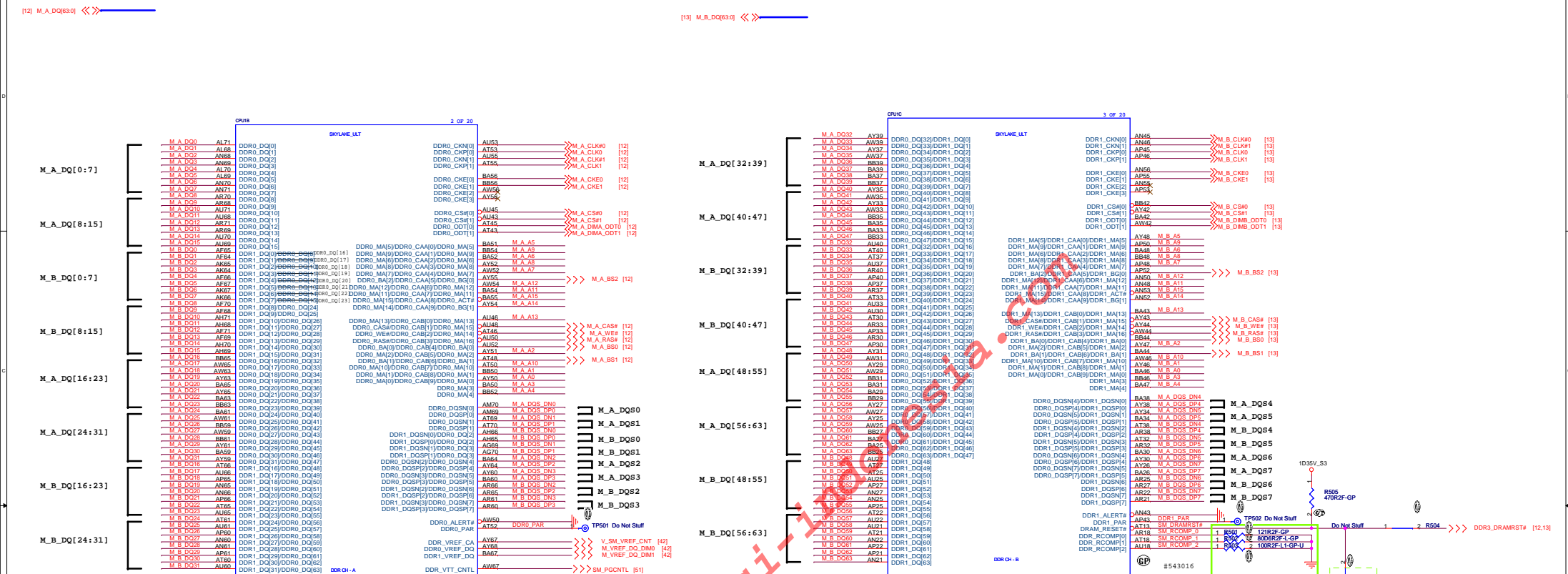
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DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

## PDG: DDR/ODT

### 4.17 SKL-U and SKL-Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

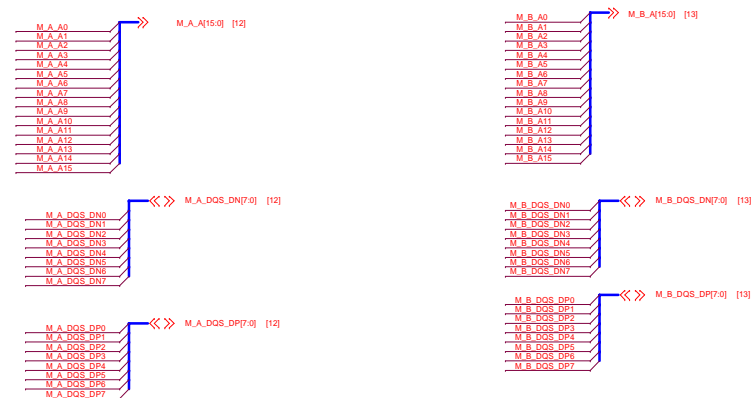
Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. Topology connection	1,2
		DRAMs	One ODT per x32 DRAM PEG Two ODT per x64 DRAM PEG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0]	Processor's ODT[1:0] connected to DRAMs' ODT. Topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PEG Two ODT per x64 DRAM PEG		
DDR3L Memory Down	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
DDR3L SO-DIMM	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs' ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
DDR3L Heat Memory Down and SO-DIMM	Processor	Processor	DDR0_ODT[1:0]	Processor's SO-DIMM Channel DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
DDR4 Memory Down	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
DDR4 SO-DIMM	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	3,4
		DIMMs	ODT[1:0]		

- Notes:
- For additional ODT signal connectivity details reference the Customer Reference Board (CRB) schematics and board files (CPUV2 - SKL-Y LPDDR3, AVP5 - SKL-U LPDDR3).
  - DDR3L Rank1 ODT is always disabled by BIOS/UEFI. ODT signal is controlling only Rank0 ODT.
  - DDR3L ODT input is held high (Active). RTT\_NORM is defined by BIOS as high-Z or both ranks, when a Rank receives write command it enables RTT\_NORM for BIOS after power training. Otherwise ODT gets RTT\_NORM high.
  - These multiselects are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 DDP dual sided and 2R x16 dual sided.

Design Guideline:  
SM\_RCMP keep routing length less than 500 mils.

Layout Note:

close to CPU



<Core Design>



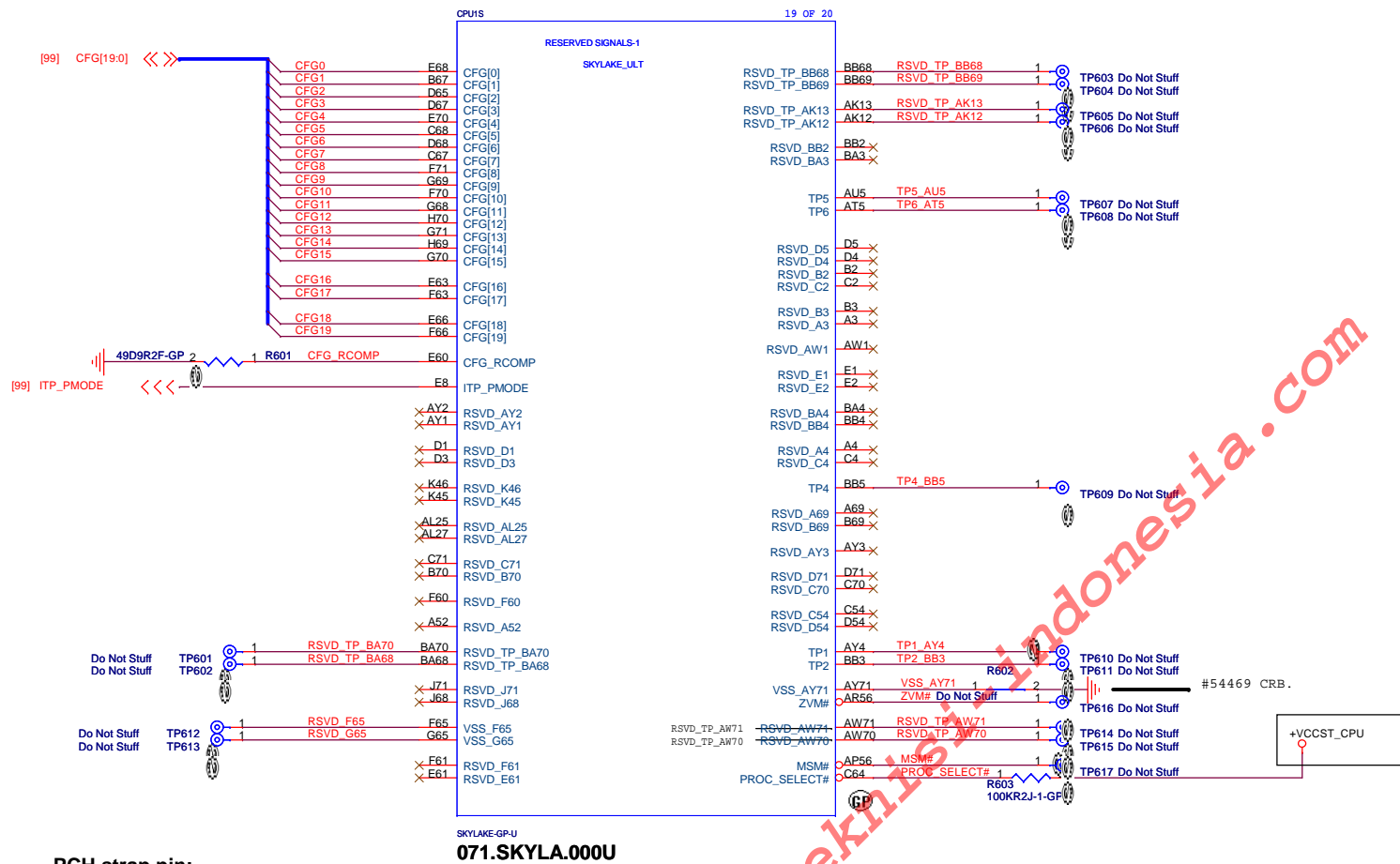
21F, 8B, Sec 1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.

File: CPU (DDR)

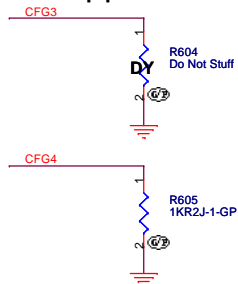
Size: A2 Document Number: Loveland SKL-U Rev: A00

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**Main Func = CPU**



**PCH strap pin:**



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort\*

## CFG TERMINATIONS

20140807 david

#544669 Rev0.52 (CRB)



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Title	Author	Year	Journal	Volume	Page
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**CPU (RESERVED)**

Size  
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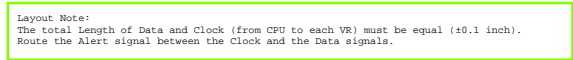
Document Number
-----------------

**Loveland SKL-U**

Rev  
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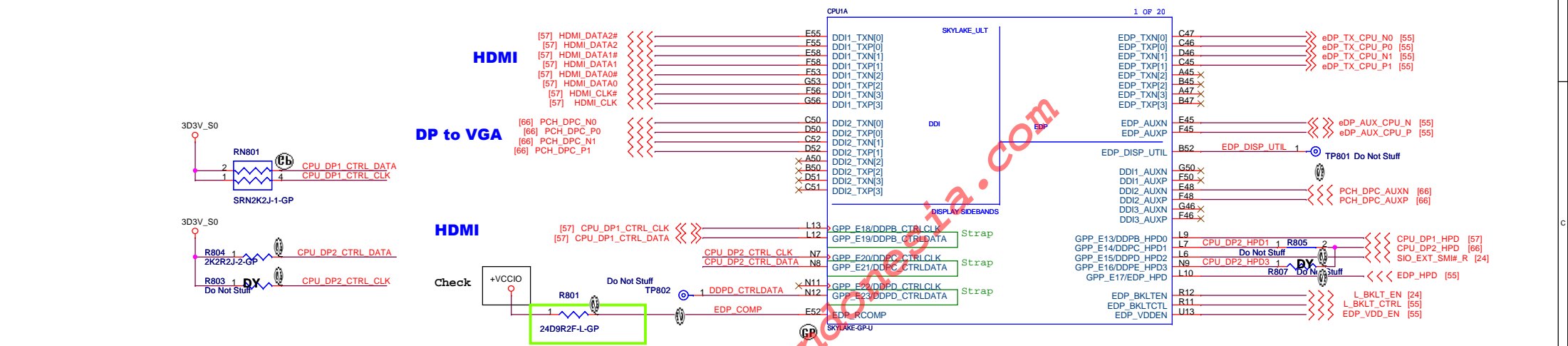
## VIDEO CLOCK



### Table 10-10.SVID Bus Routing Guidelines



impedance=50 ohm  
3. Length match<25mil



(#543016) eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 $\Omega$ $\pm$ 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm$ 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm$ 5% resistor	NC

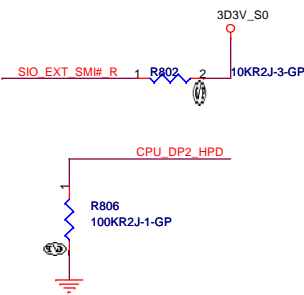
Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.  
Design Guideline:  
Skylake processor signal eDP\_RCOMP should be connected to the VCCIO rail via a single 24.9  $\pm$ 1%  $\Omega$  resistor.

071.SKYLA.000U

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.






Main Func = CPU

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### Table 53-3. SKL U Bulk Decoupling Requirements

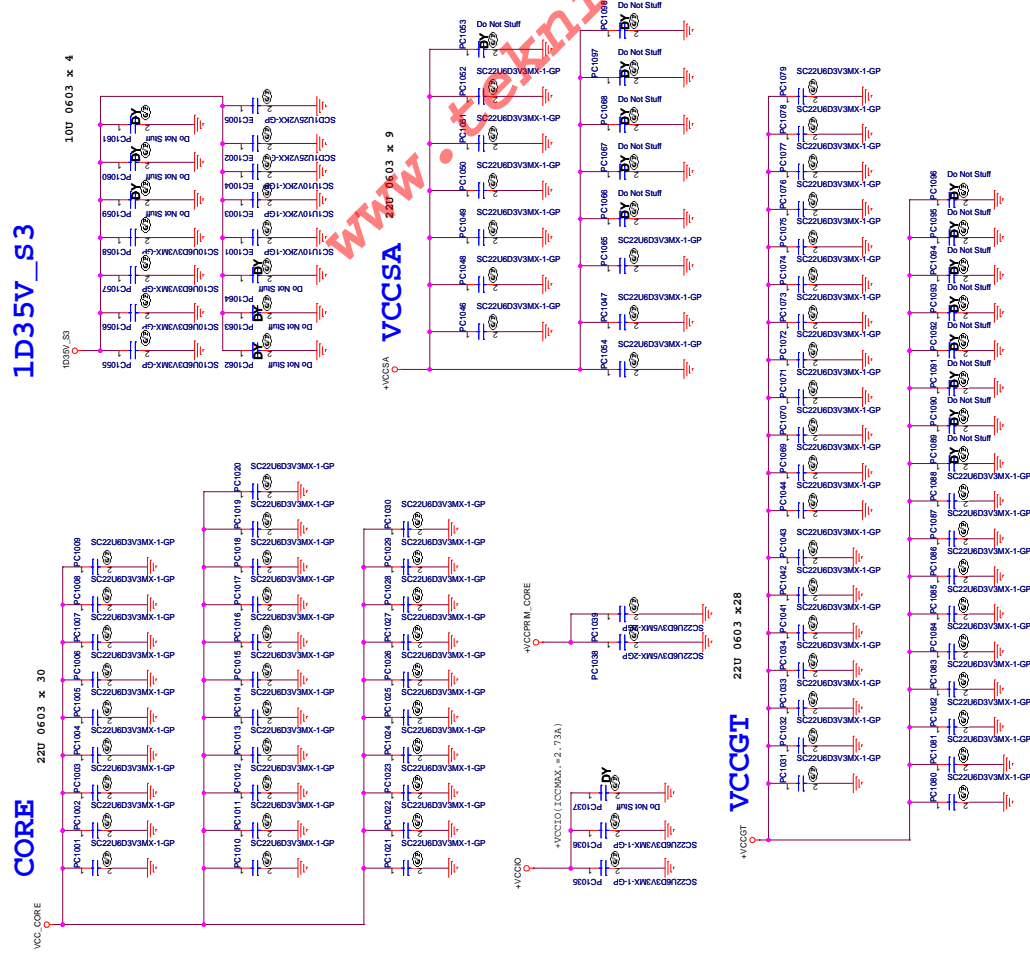
Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output
	1x 220µF (0.4-5mΩ ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output
	1x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGT <sub>1</sub> Power Plane at VR output	1x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47µF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47µF 0805	Placed at primary side near to VR output

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

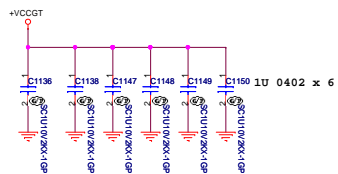
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V) <sup>1</sup>	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
			Only needed when supporting 23e
VCCSA		8x 22uF 0603	Only needed when supporting 23e
	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
VDDQ		4x 1uF 0402	Place as close to the package as possible
	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
VDDPC		4x 10uF 0402	Place as close to the package as possible
	1x 1uF 0201		Place on secondary side, underneath the package
VCCPL		1x 1uF 0402	Place as close to the package as possible
		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

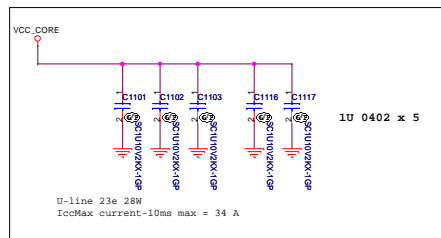
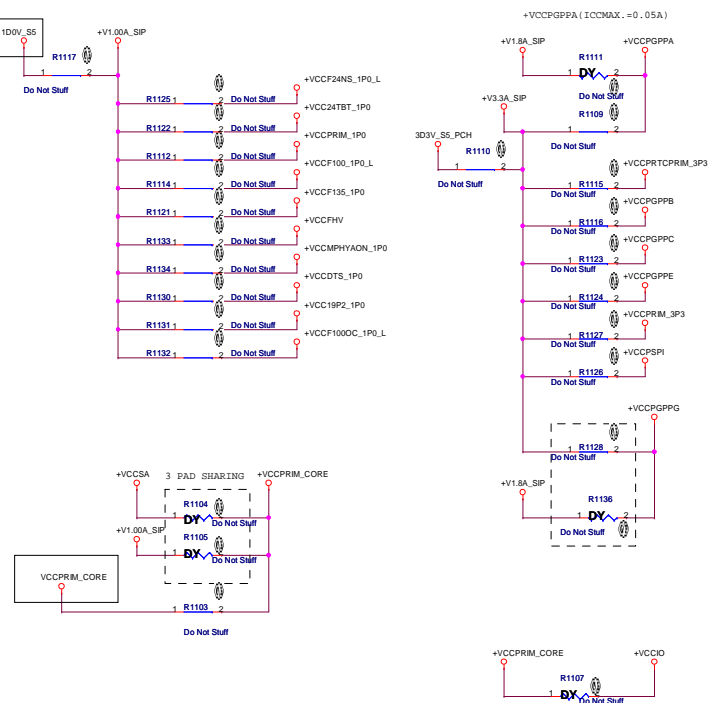
Domain	Backfile cap	Primary side cap	Placement guideline
VCCSTG	1x 1UF 0402		Place on secondary side, underneath the package Placeholder only
VCCOEPI0	2x 10UF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10UF 0402 6x 1UF 0201		Place on secondary side, underneath the package



# Main Func = CPU



## PCH DERIVED RAILS



## VCCIO

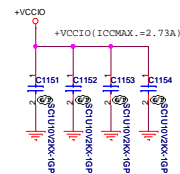
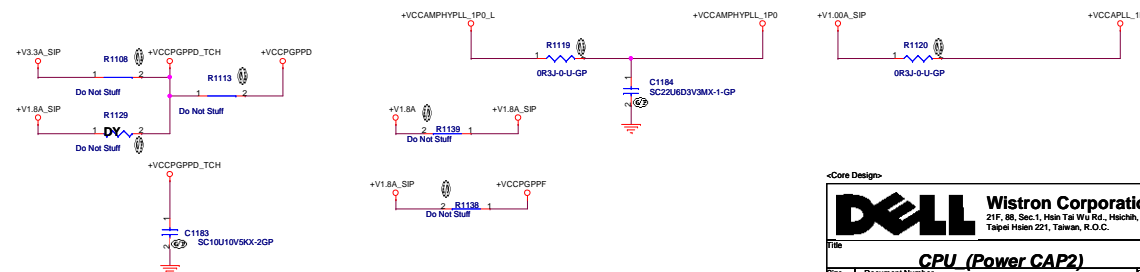
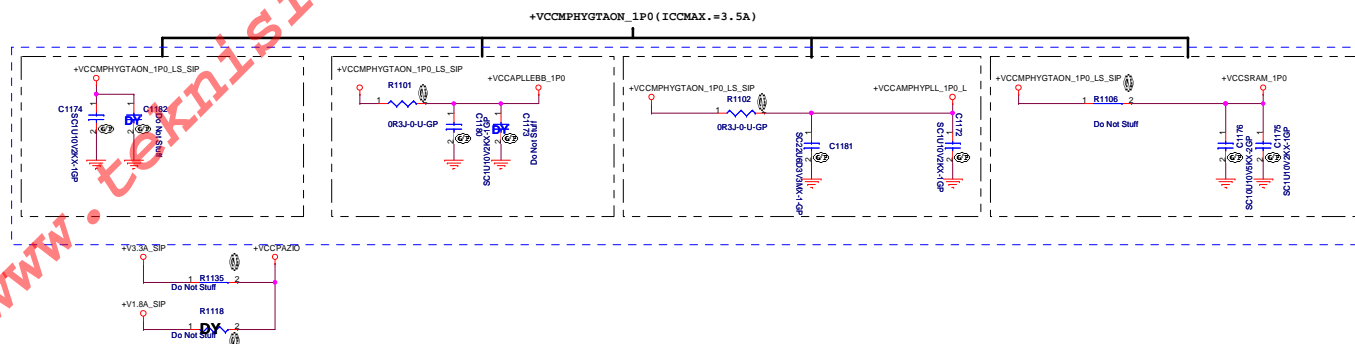


Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201	(6.3V)*	
VCCGT	10x 10uF 0402	8x 10uF 0402	Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0905 (6.3V)*	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible



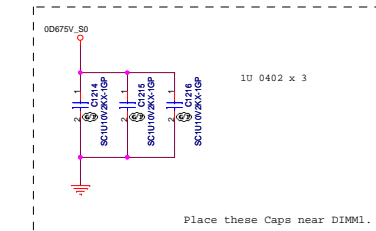
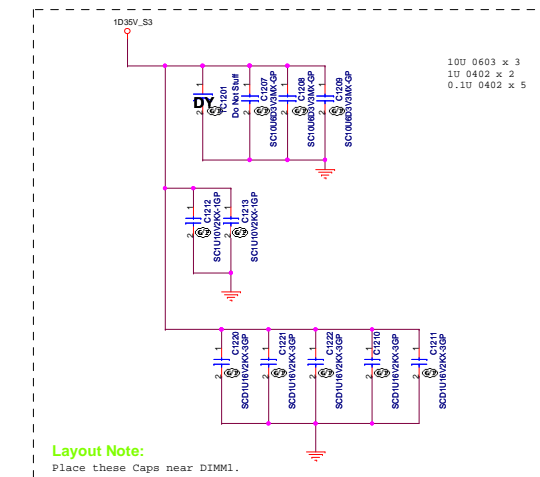
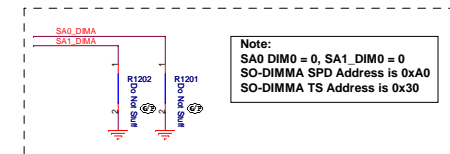
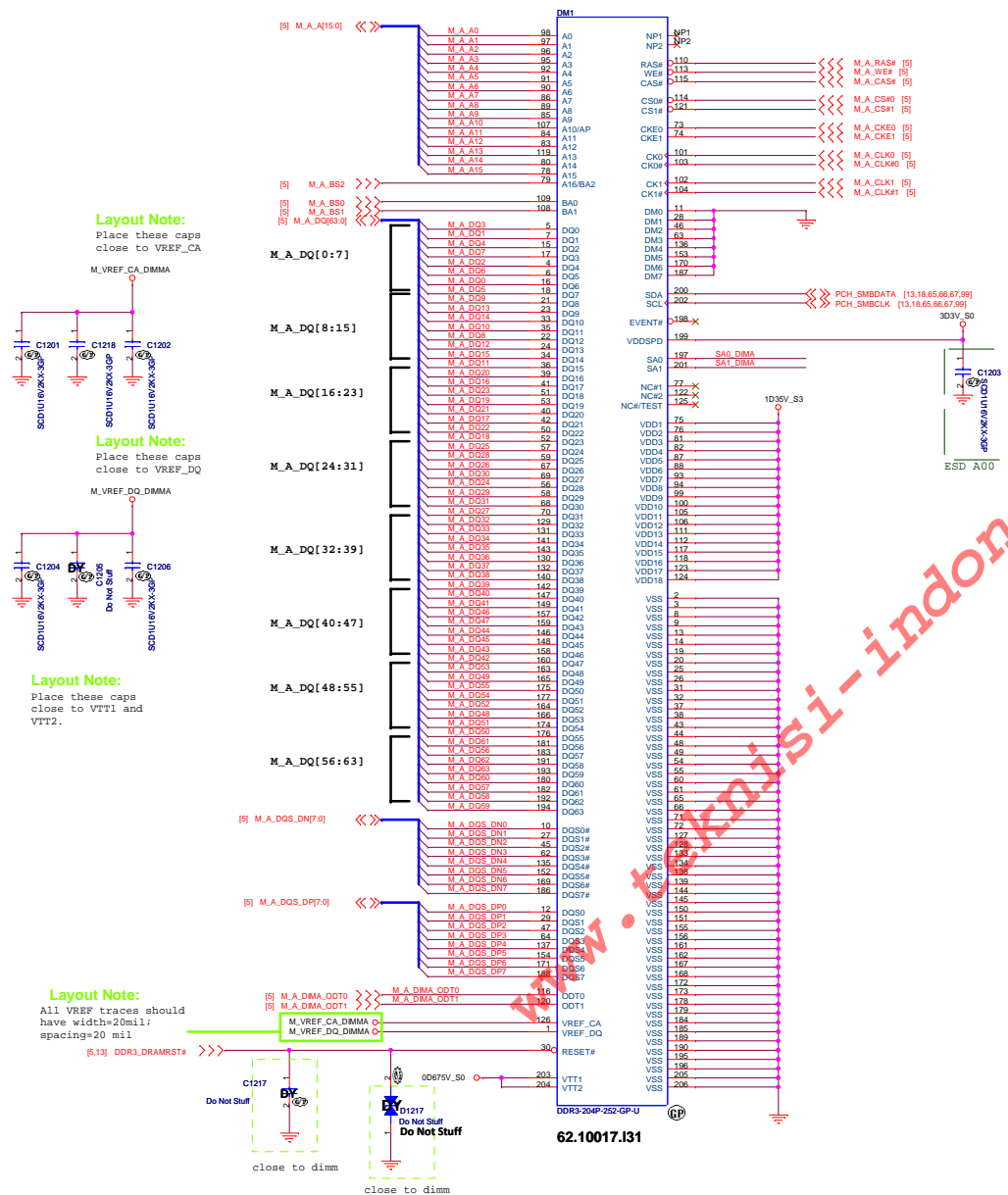
<Core Design>

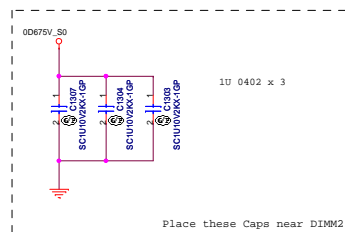
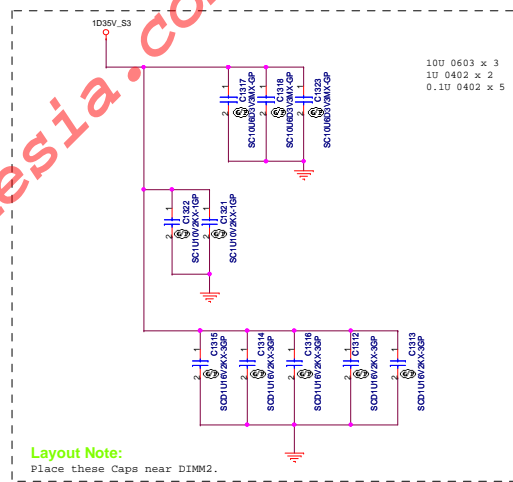
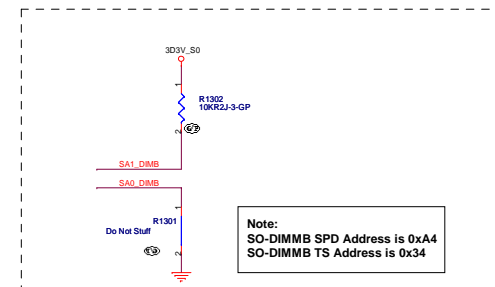
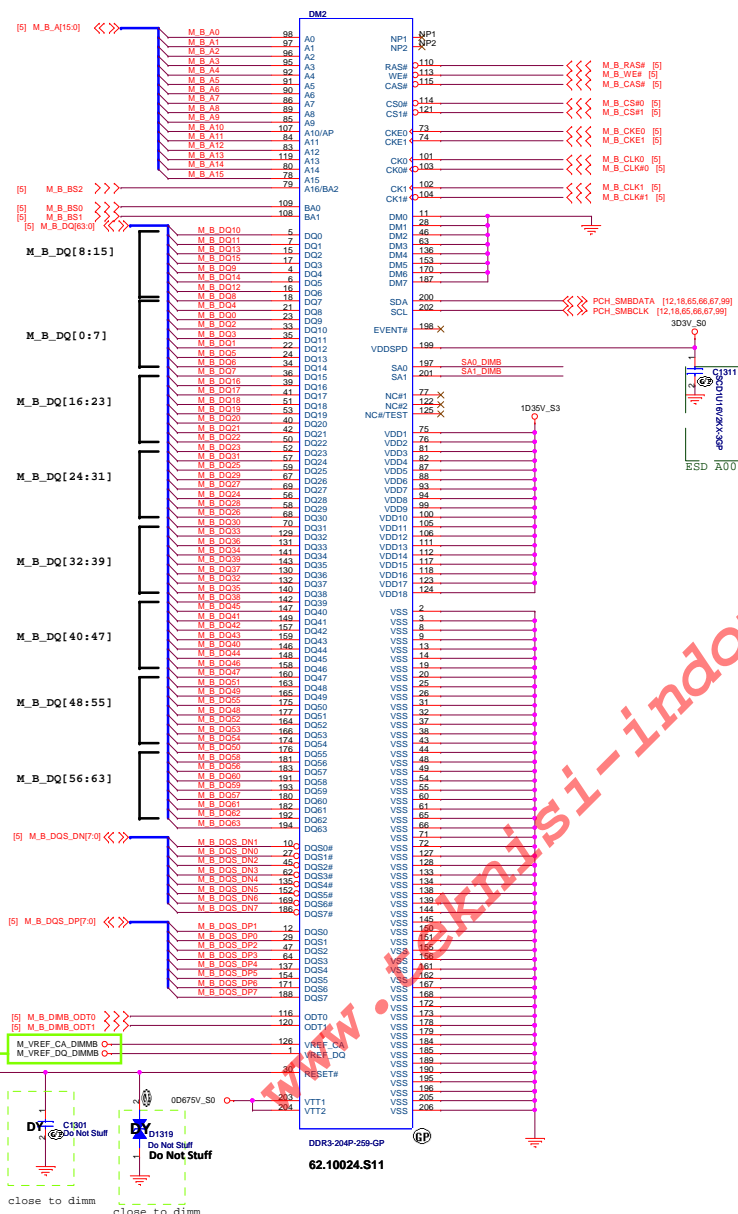
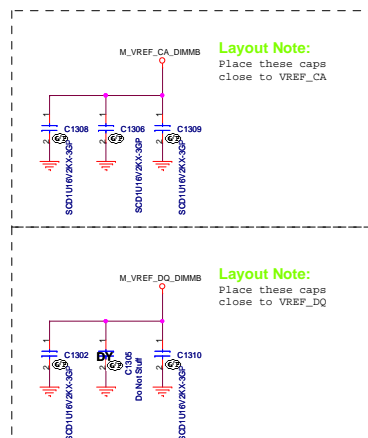
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**CPU (Power CAP2)**

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Size A4		Document Number <b>Loveland SKL-U</b>			Rev <b>A00</b>
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Main Func = PCH

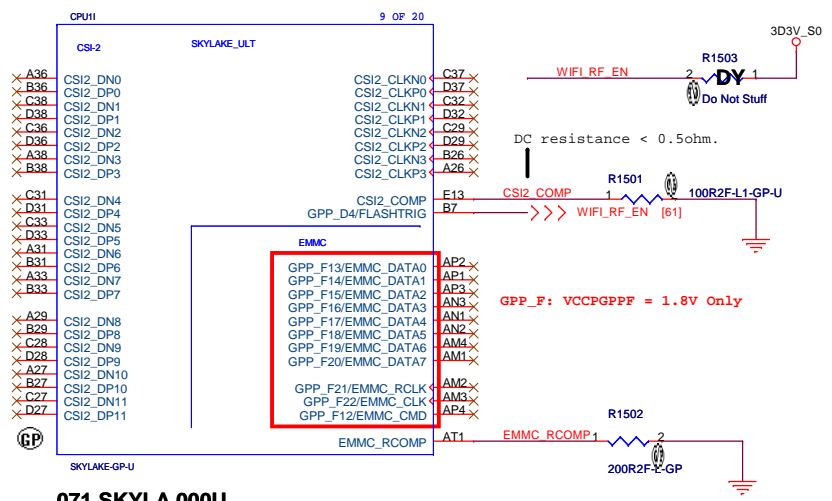


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

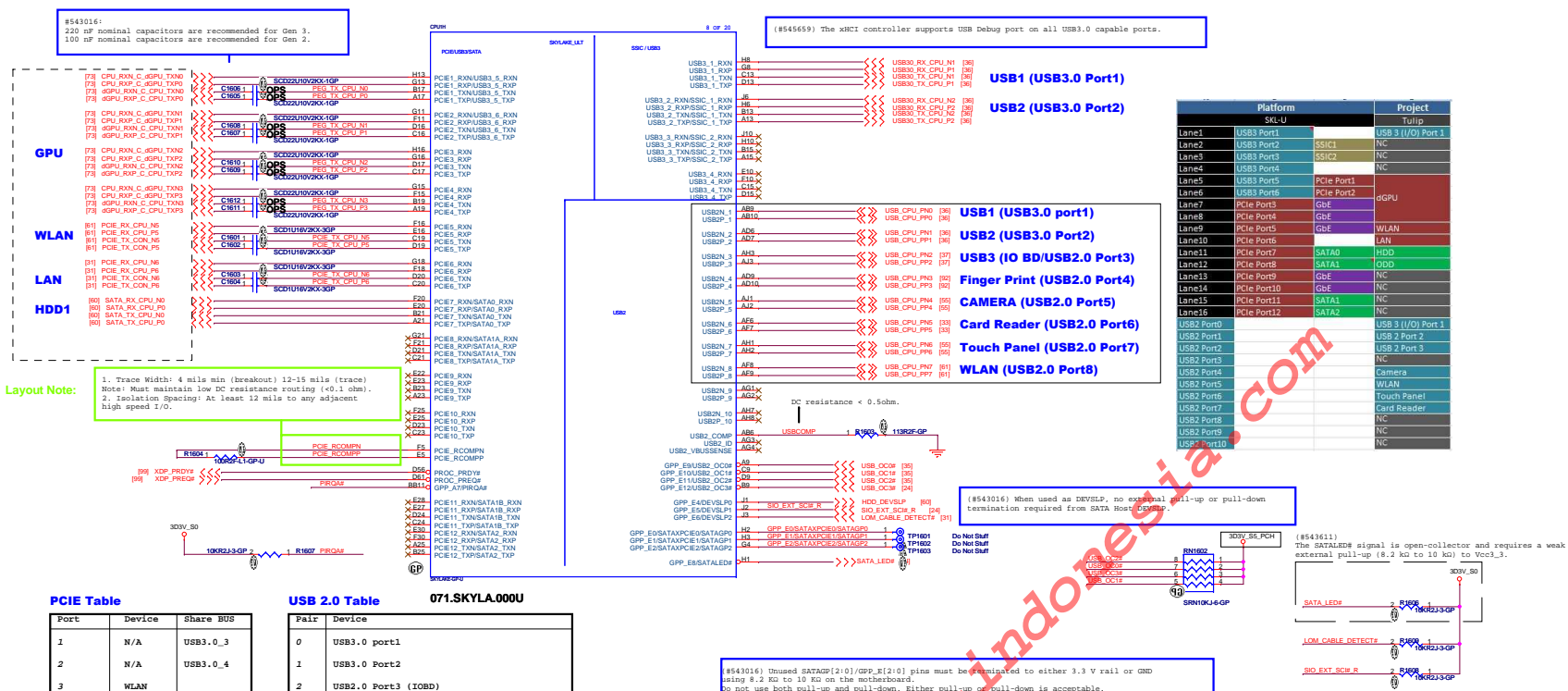
[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



Main Func = PCH



**PCIe Table**

Port	Device	Share BUS
1	N/A	USB3_0_3
2	N/A	USB3_0_4
3	WLAN	
4	LAN	
5 (L0-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	N/A	
6 (L0-L1)	N/A	

**USB 2.0 Table**

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOBD)
3	Finger print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

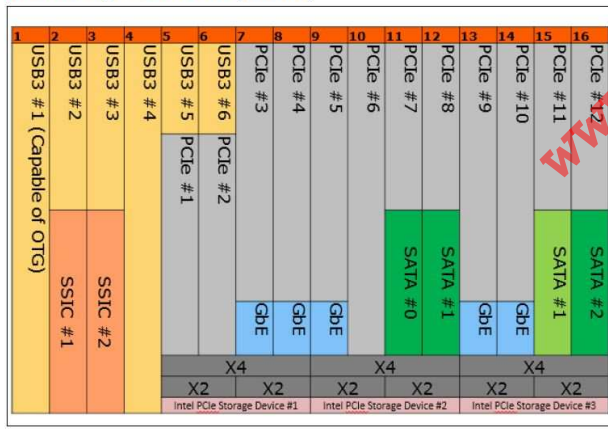


Table 24-2. PCI Express\* Port Feature Details

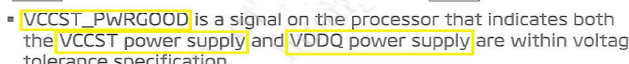
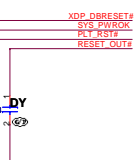
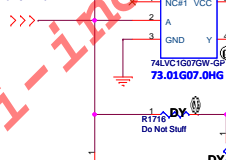
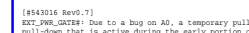
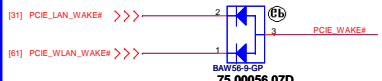
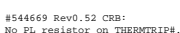
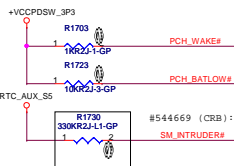
SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express\* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x4	Port1				Port5							
Y	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9		Port10	



**ln Func = PCH**



1. VCCST\_PWRGD is only 1.0 V tolerant.
2. VCCST\_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST.



# Main Func = PCH

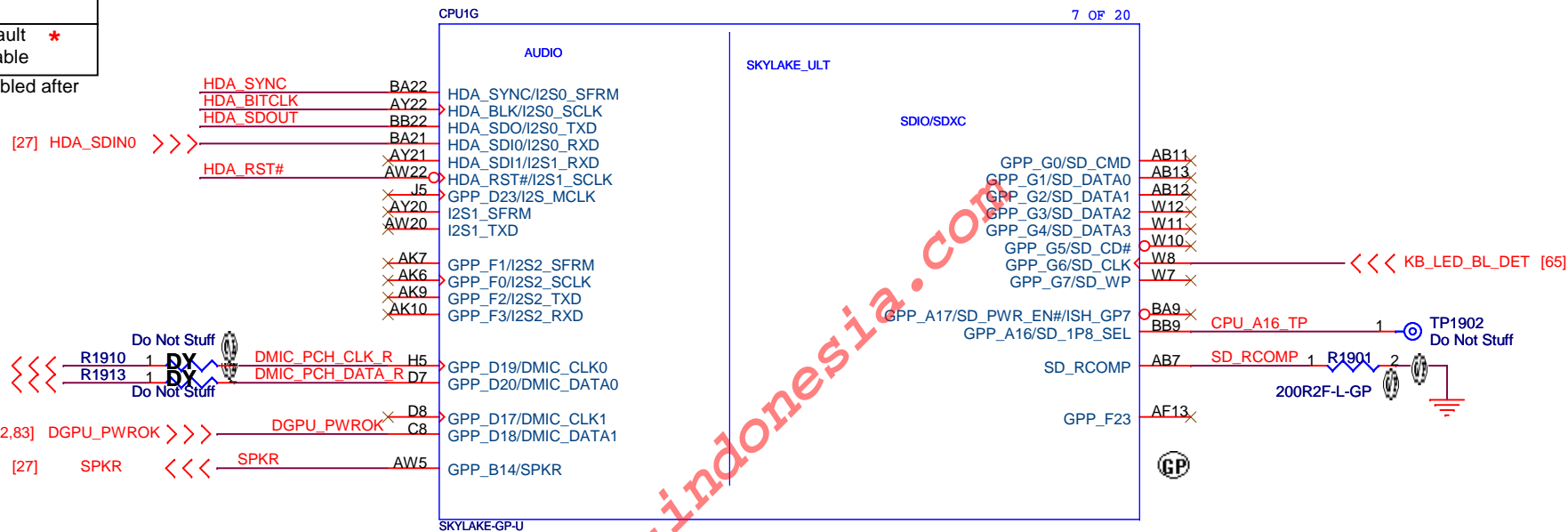
## PCH strap pin:

Flash Descriptor Security Override/  
Intel ME Debug Mode

HDA\_SDOUT

Low = Default \*  
High = Enable

The internal pull-down is disabled after  
PLTRST# deasserts



071.SKYLA.000U

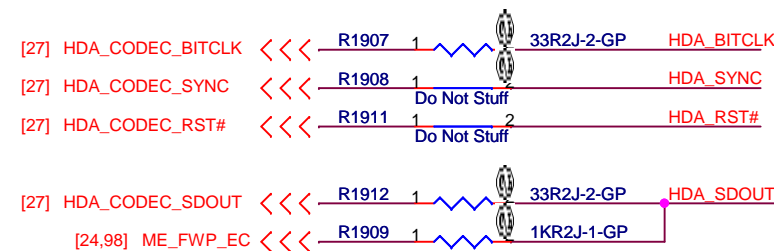
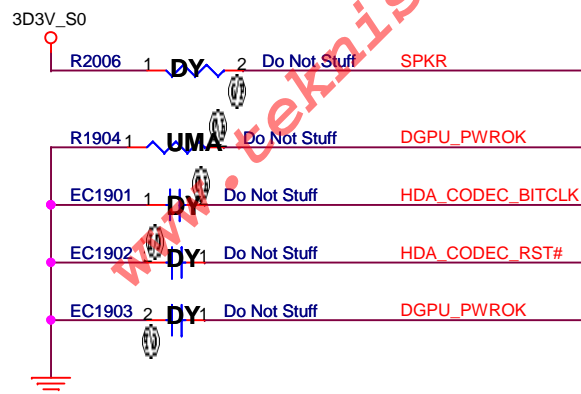
## PCH strap pin:

NO REBOOT

HDA\_SPKR

\* Low = Enable (Default)  
High = Disable

The internal pull-down is disabled after  
PLTRST# deasserts



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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (AUDIO/SDIO/SDXC)

Size  
A4

Document Number

Loveland SKL-U

Rev  
A00

Date: Tuesday, September 15, 2015

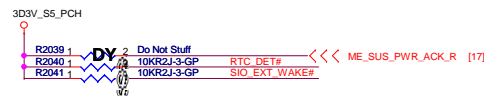
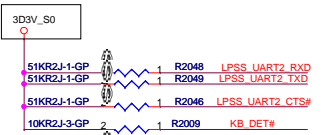
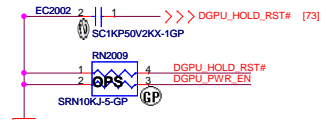
Sheet 19 of 105

Main Func = PCH

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPH1_MOSI / GPP_B22	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10      Boot BIOS Destination 0            SPI 1            LPC

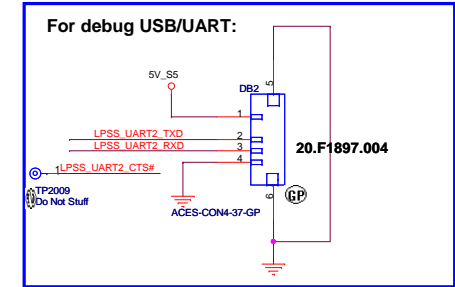
The signal has a weak internal pull-down.



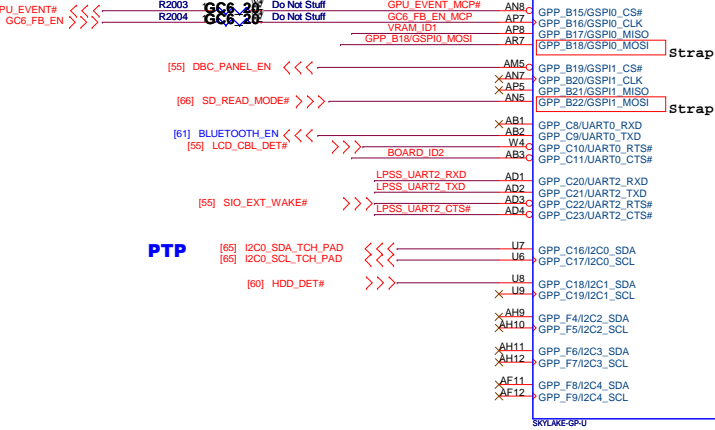
PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPH1_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

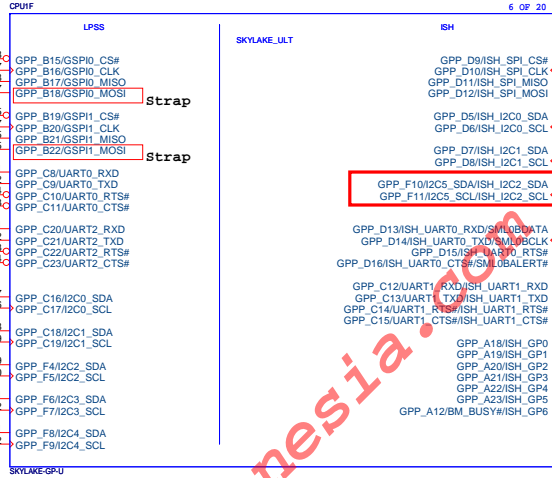
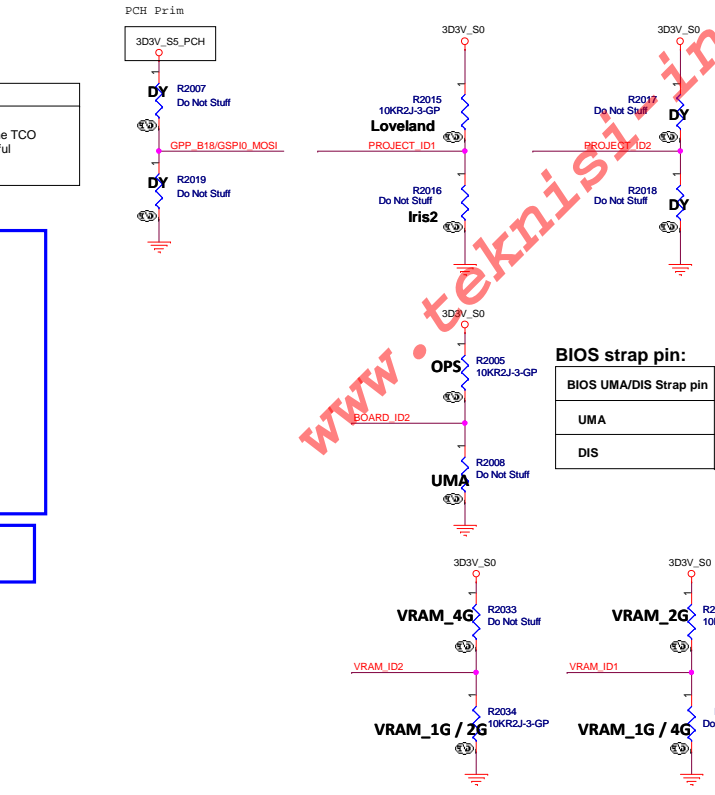
The signal has a weak internal pull-down.



Intel has removed EHCI controller from BDW and proposed to use UART interface for Win7 debug.



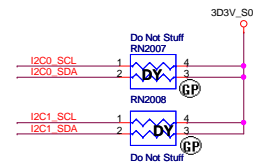
PCH Prim



071.SKYLA.000U

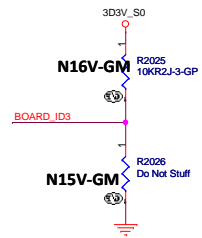
BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2	PROJECT_ID1
Iris2	0	0
Loveland	0	1
Tulip	0	0



BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

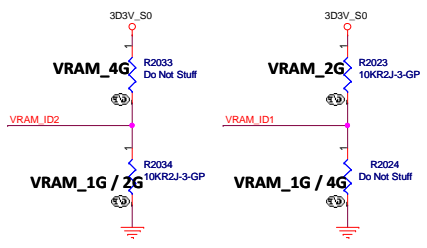


BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM-S	0
N16V-GM	1

BIOS strap pin:

BIOS VRAM Size Strap pin	VRAM_ID2	VRAM_ID1
1G	0	0
2G	0	1
4G	1	0

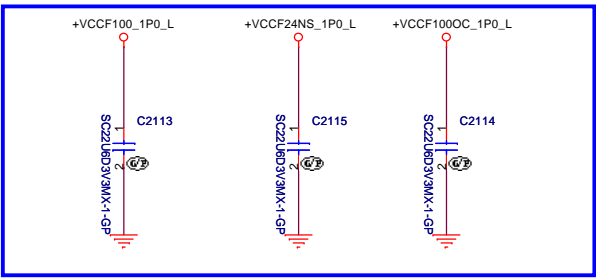
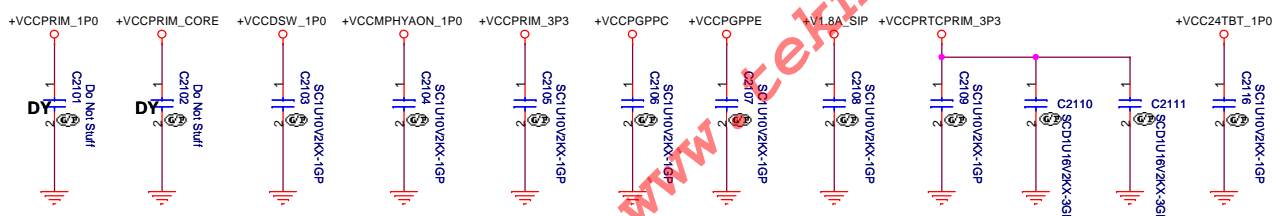
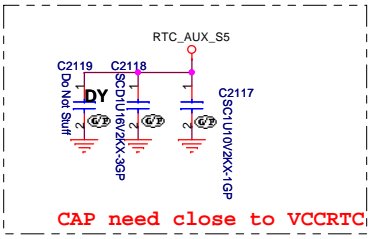
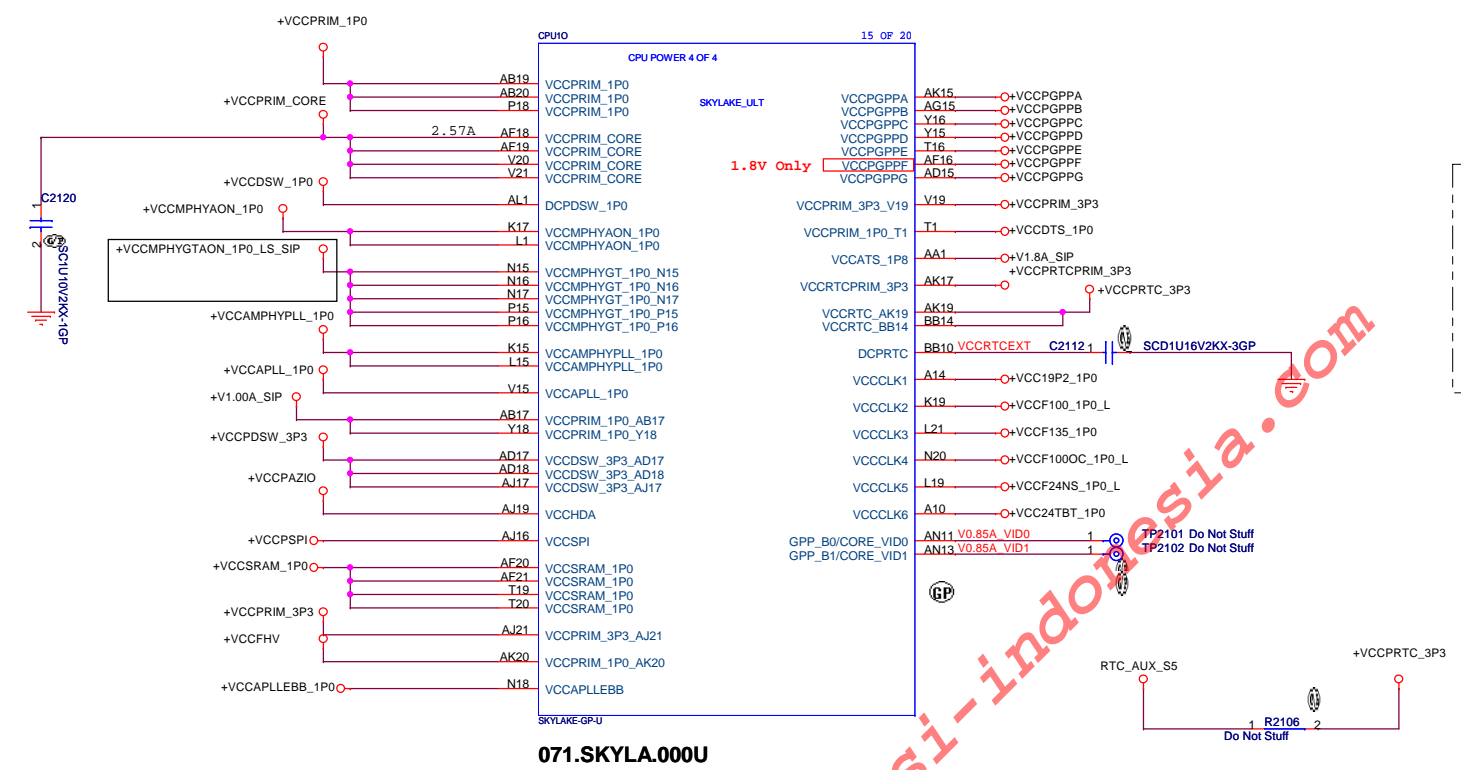


(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

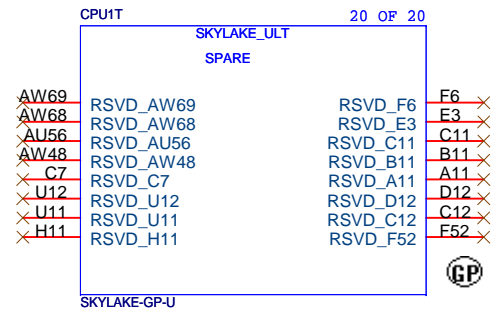
1.8v Only

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

Main Func = PCH




Main Func = PCH



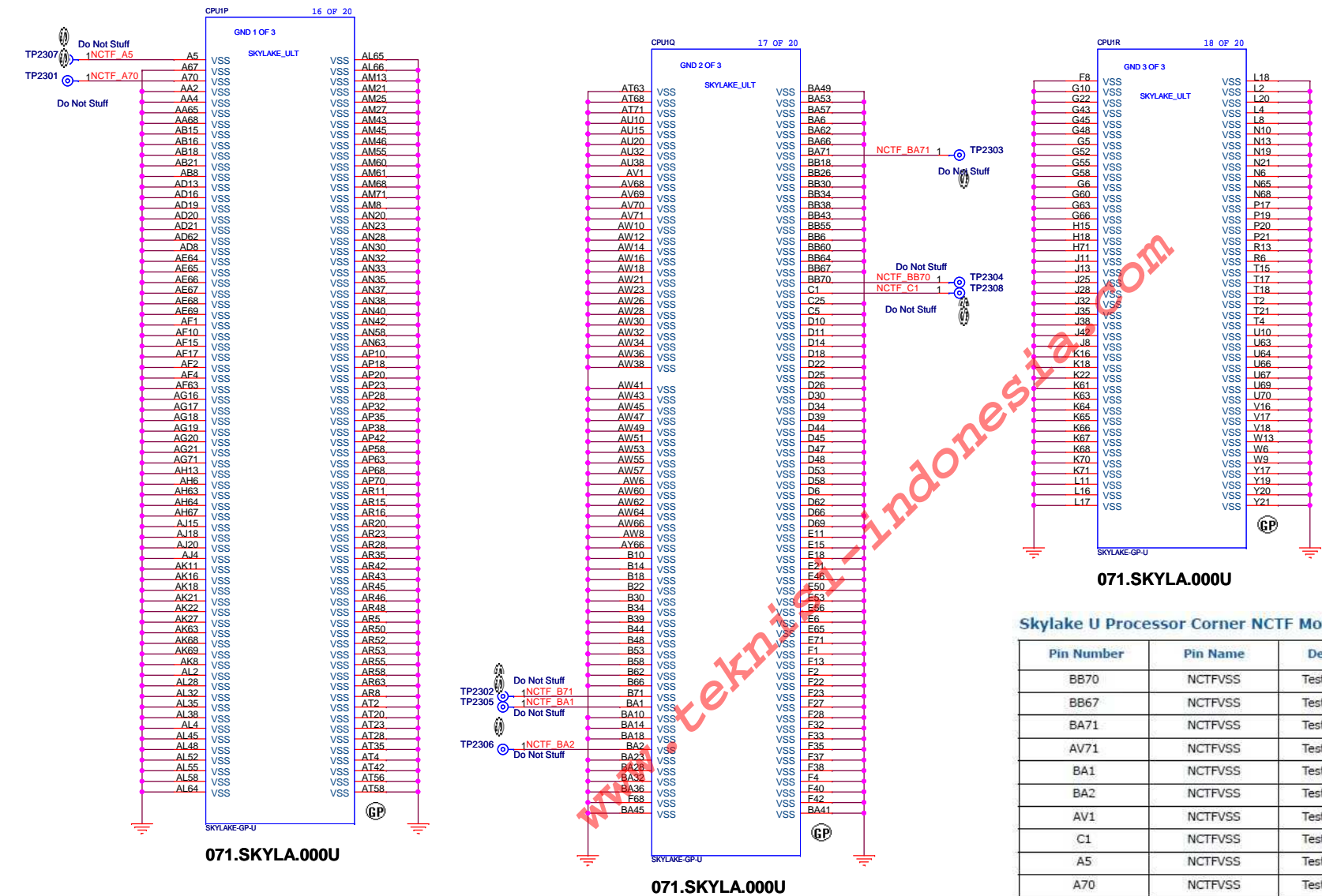
071.SKYLA.000U

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CPU (RSVD)</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
Date: Tuesday, September 15, 2015		Sheet 22 of	105


Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (VSS)**

Size

Document Number

Rev

A3

**Loveland SKL-U**

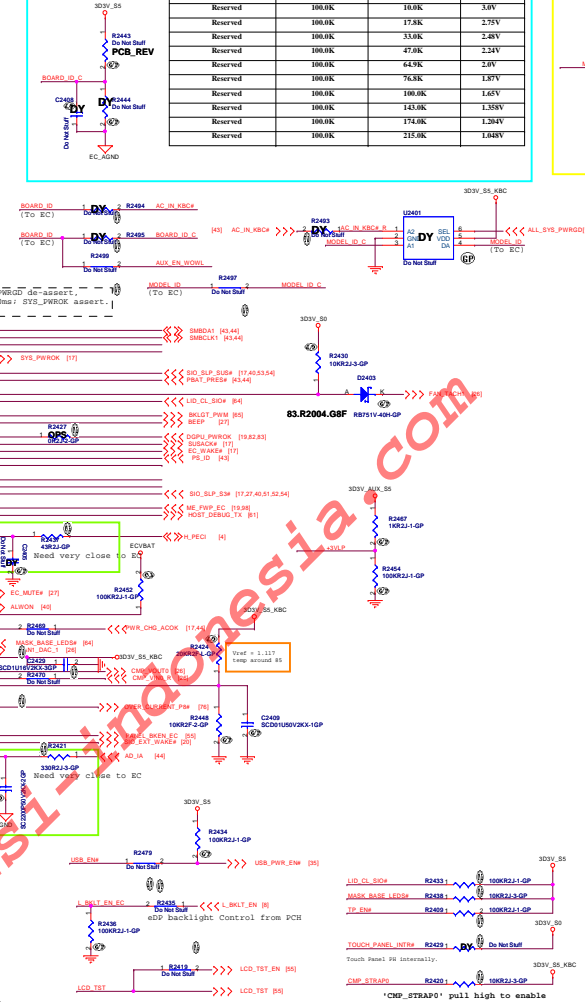
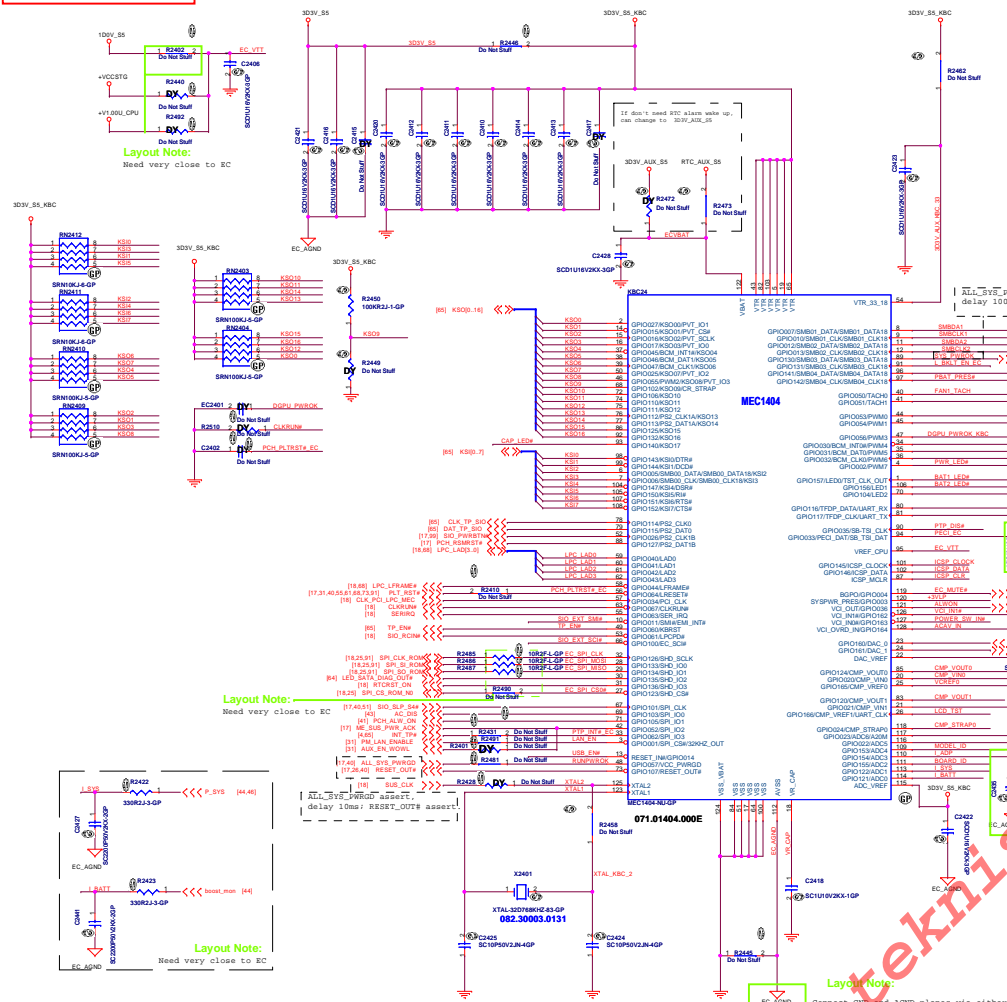
**A00**

Date: Tuesday, September 15, 2015

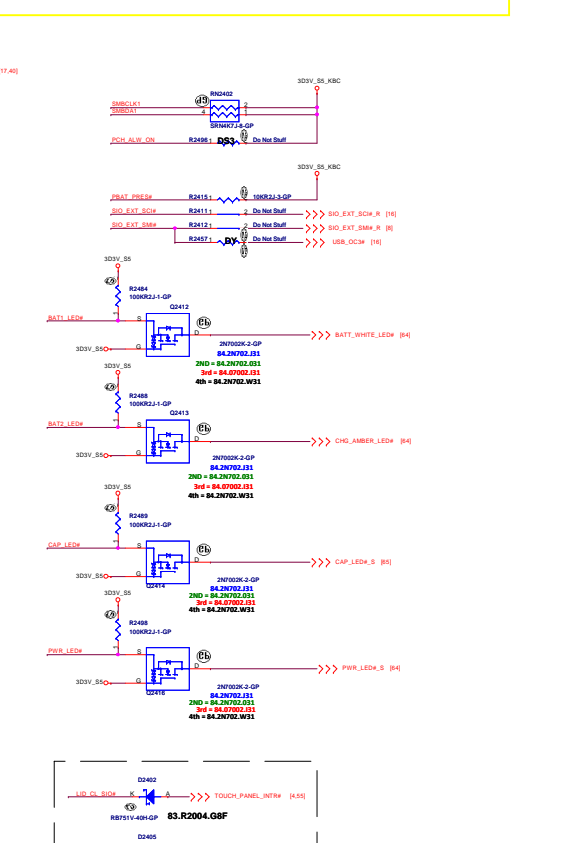
Sheet 23 of 105



Main Func = KBC



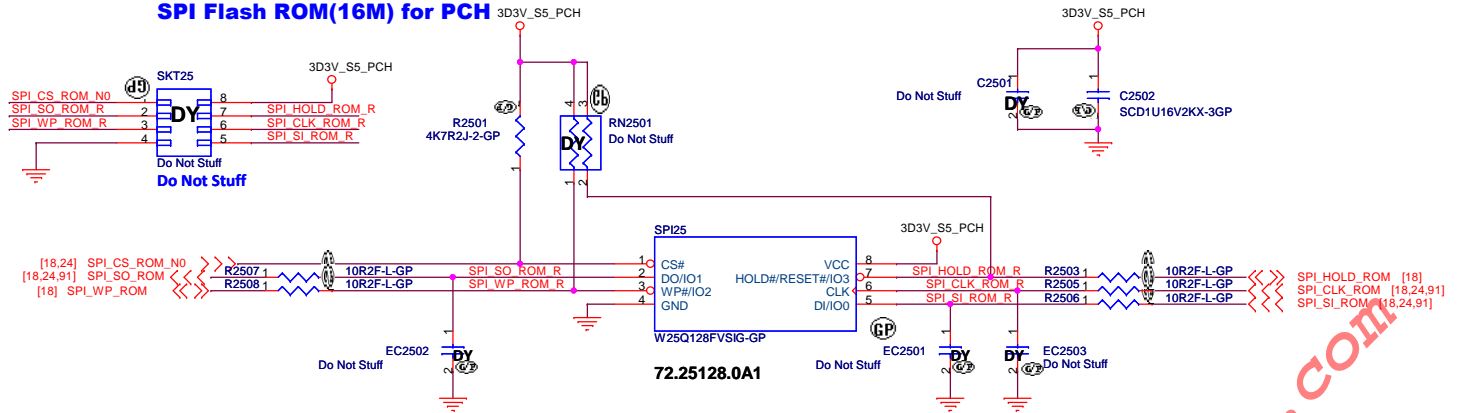
MODE_ID	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Low-imp. (VMA_VBI)	100.0k	4.75k/64.4k/92.5k/40k	3.14V
Low-imp. (VMA_VBI)	100.0k	1k/26.6k/4.64k/52k/40k	2.84V
Low-imp. (VMA_VBI)	100.0k	2k/26.6k/4.64k/52k/40k	2.84V
Reserved	100.0k	100.0k/4.75k/40k/92.5k/40k	2.87V
Reserved	100.0k	100.0k/4.75k/40k/92.5k/40k	2.87V
Low-imp. (VBI_VBI)	100.0k	100.0k/4.75k/40k/92.5k/40k	2.87V
Low-imp. (VBI_VBI)	100.0k	100.0k/4.75k/40k/92.5k/40k	2.87V
Reserved	100.0k	100.0k/4.75k/40k/92.5k/40k	2.87V
Reserved	100.0k	100.0k/4.75k/40k/92.5k/40k	2.87V



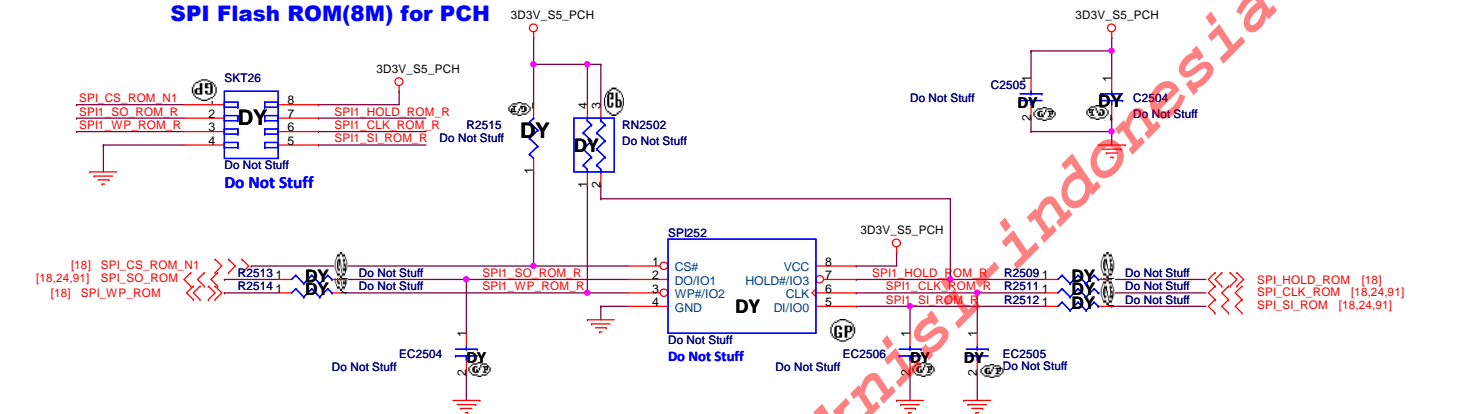


Main Func = SPI Flash

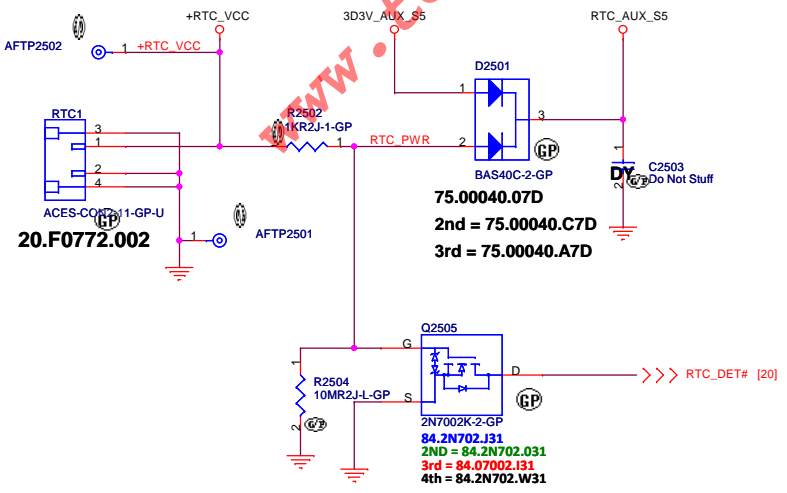
SPI Flash ROM(16M) for PCH



SPI Flash ROM(8M) for PCH



Main Func = RTC








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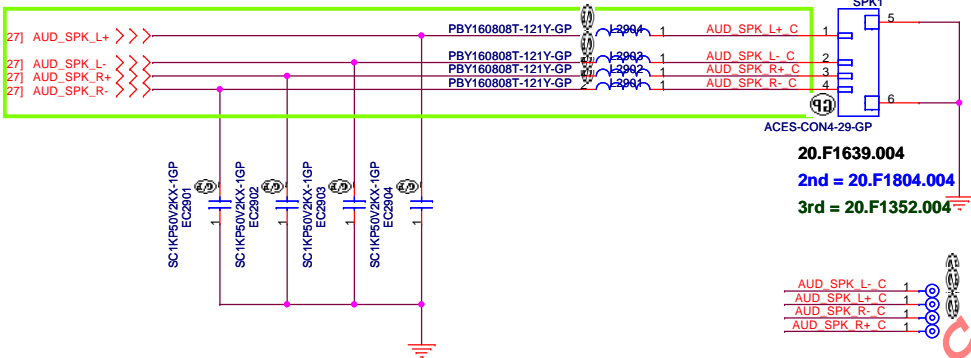
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
Date: Tuesday, September 15, 2015		Sheet 28 of	105

Main Func = Audio

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



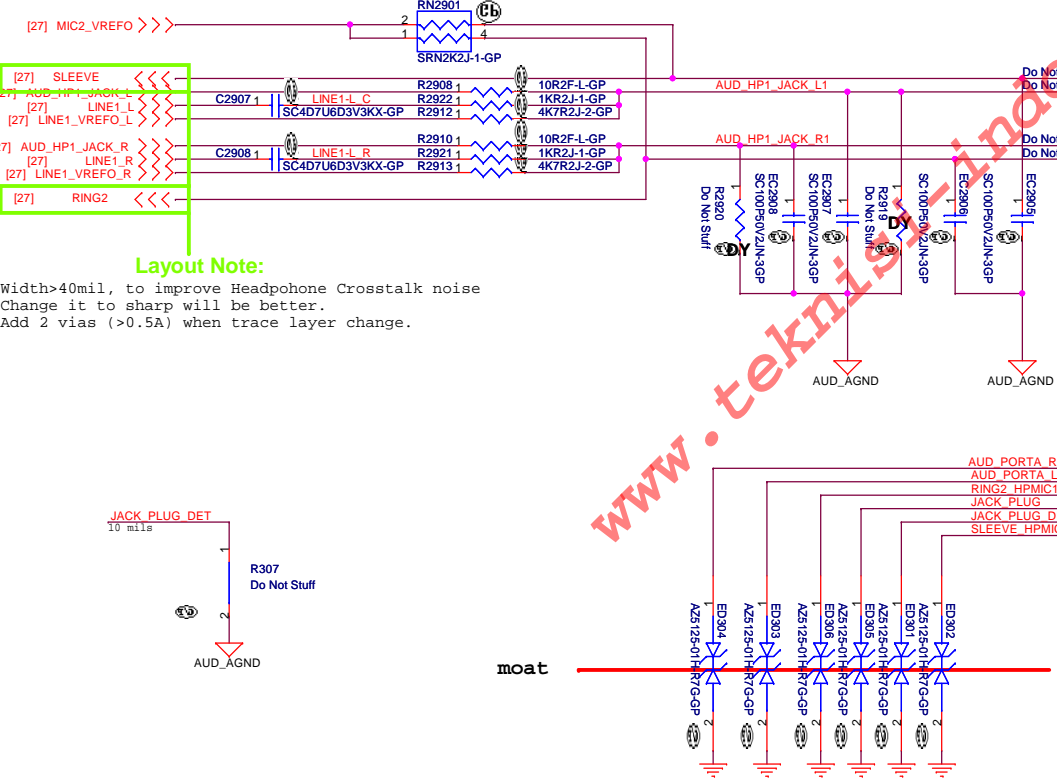
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

AUD\_SPK\_L- C 1  
AUD\_SPK\_L+ C 1  
AUD\_SPK\_R- C 1  
AUD\_SPK\_R+ C 1

20.F1639.004  
2nd = 20.F1804.004  
3rd = 20.F1352.004

Layout Note:

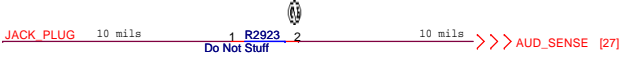
Width>40mil, to improve Headphone Crosstalk noise  
Change it to sharp will be better.  
Add 2 vias (>0.5A) when trace layer change.



A00 08/17



Shift Issue  
PAD-AUDIO-JK509-GP-U-1  
ZZ.00PAD.IB1  
HPMIC1  
Main Source : 022.10002.0981  
2nd : 022.10002.00D1  
3rd : 022.10002.00P1




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Main Func = Audio

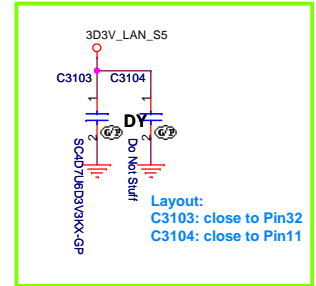
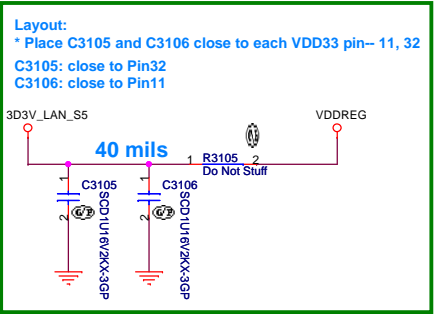
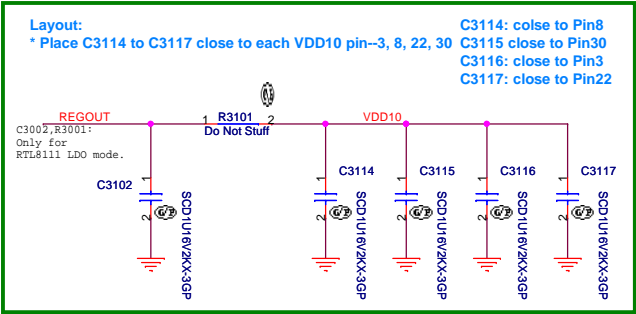
(Blanking)

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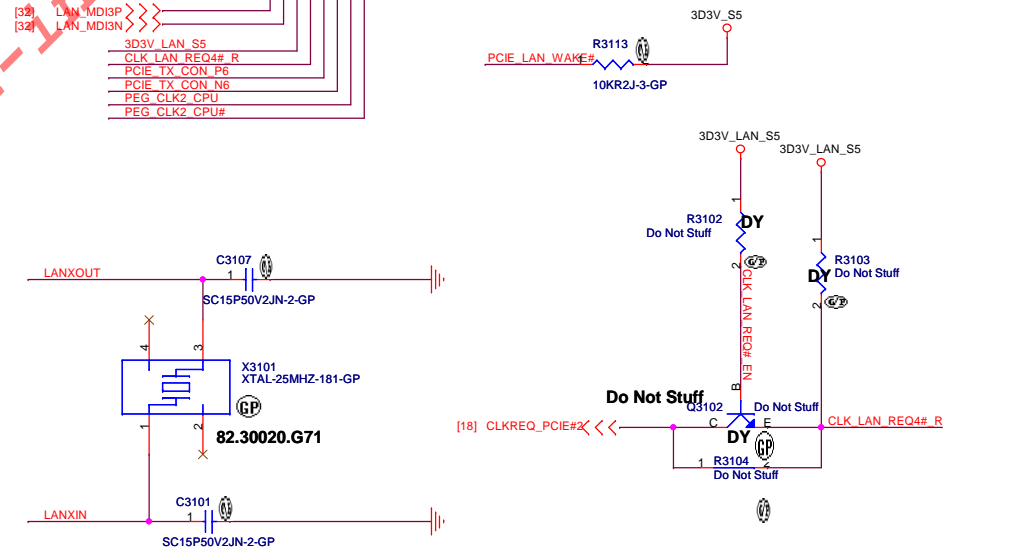
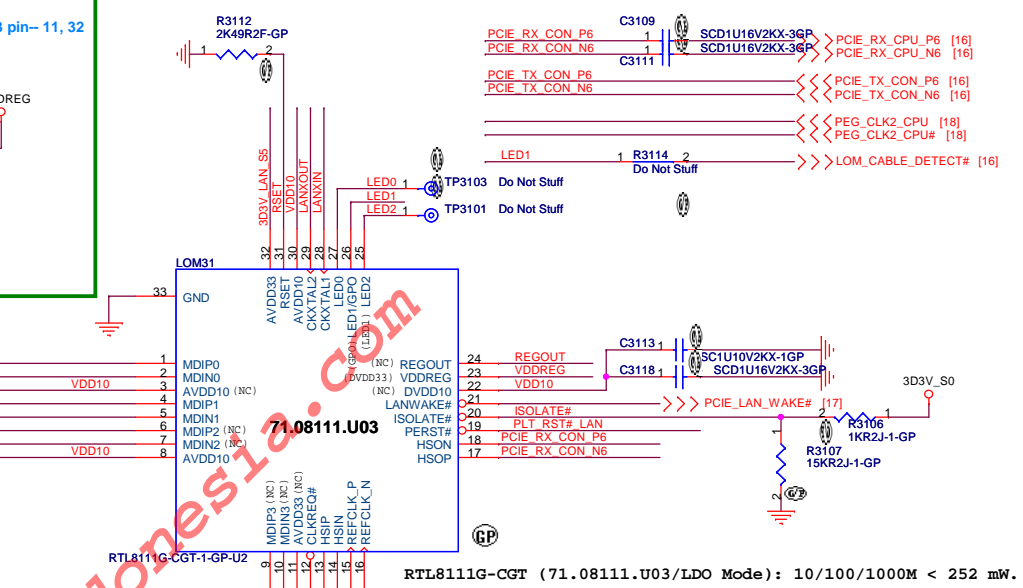
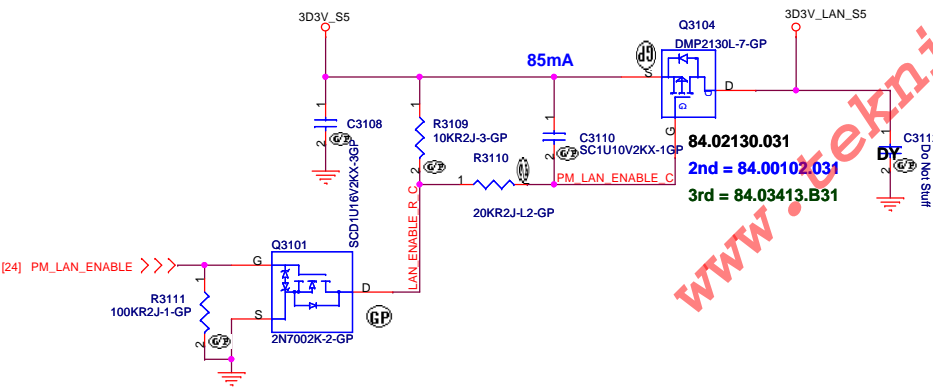
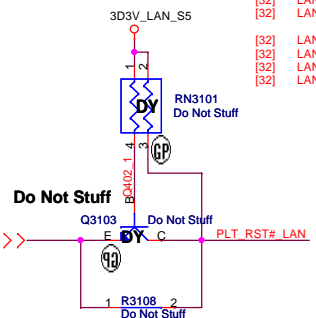
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
Date: Tuesday, September 15, 2015		Sheet 30 of 105	

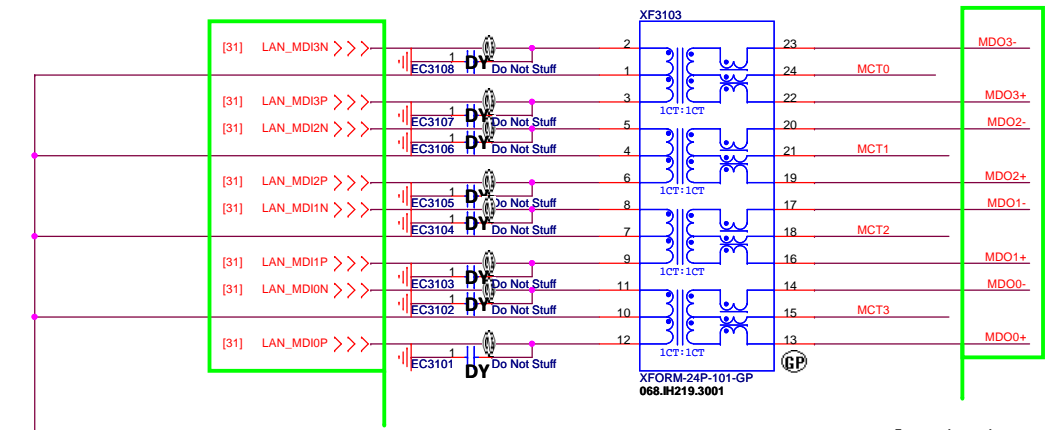
Main Func = LAN



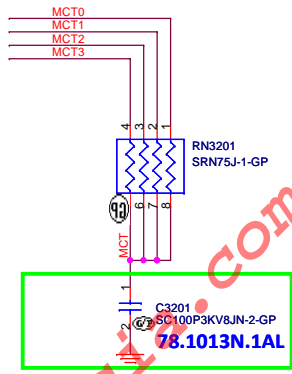
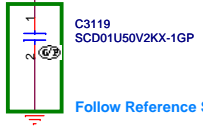
3D3V\_LAN\_S5 rise time must be controlled between 0.5 mS and 100 mS.



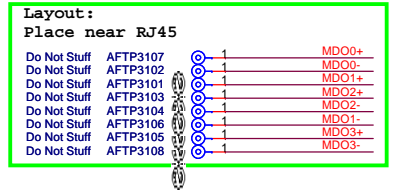
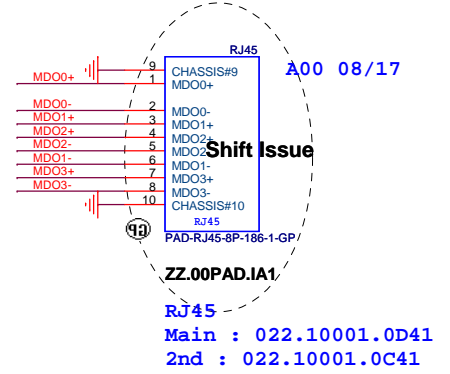
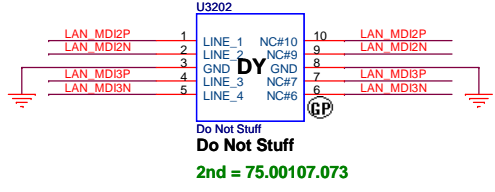
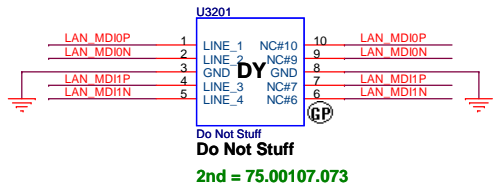
LAN TransFormer (10/100/1000M)



Layout note:  
30 mil spacing between MDI differential pairs.

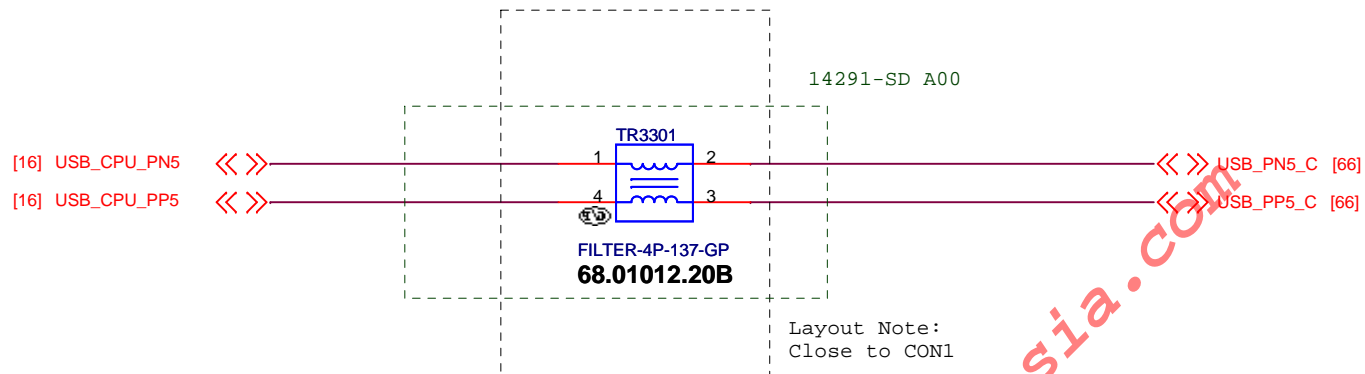


Layout note:  
30 mil spacing between MDI differential pairs.





Main Func = Card Reader



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Card Reader-RTS5170**

Size  
A4

Document Number

**Loveland SKL-U**

Rev  
A00

Date: Tuesday, September 15, 2015


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Main Func = USB3.0 Port1

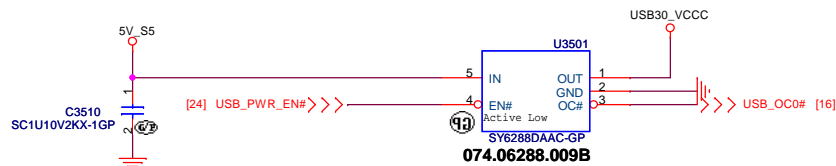
(Blanking)

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<Core Design>

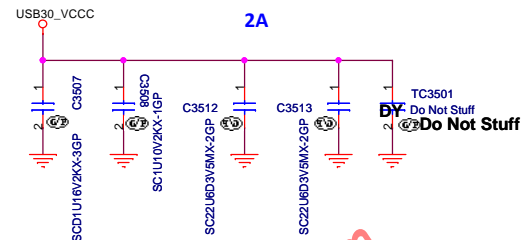
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
Date: Tuesday, September 15, 2015		Sheet 34 of	105

## Main Func = USB3.0 Port1

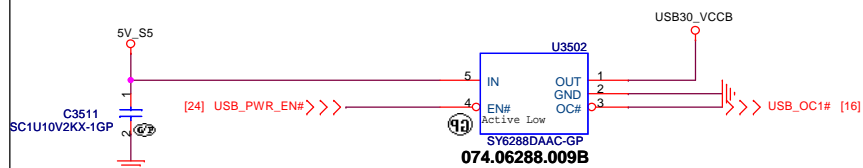


### USB3.0 Port1

Layout Note: Close USB1

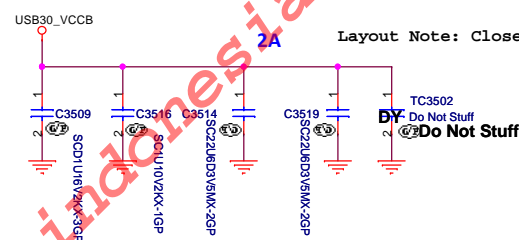


## Main Func = USB3.0 Port2

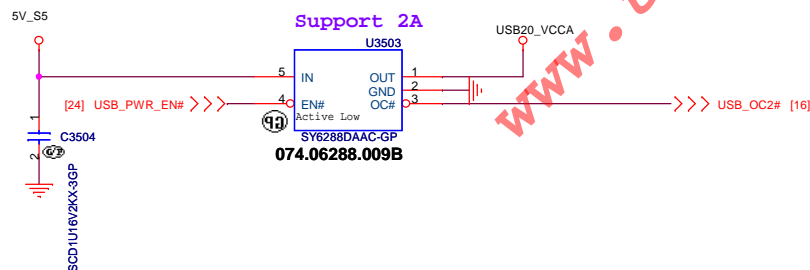


### USB3.0 Port2

Layout Note: Close USB2

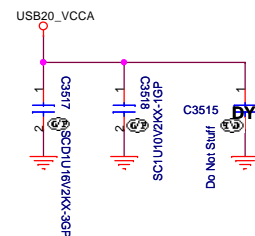


## Main Func = USB2.0 Port3



### USB2.0 Port3 (IO Board)

Layout Note: Close CON1



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB switch**

Size Document Number

**Loveland SKL-U**

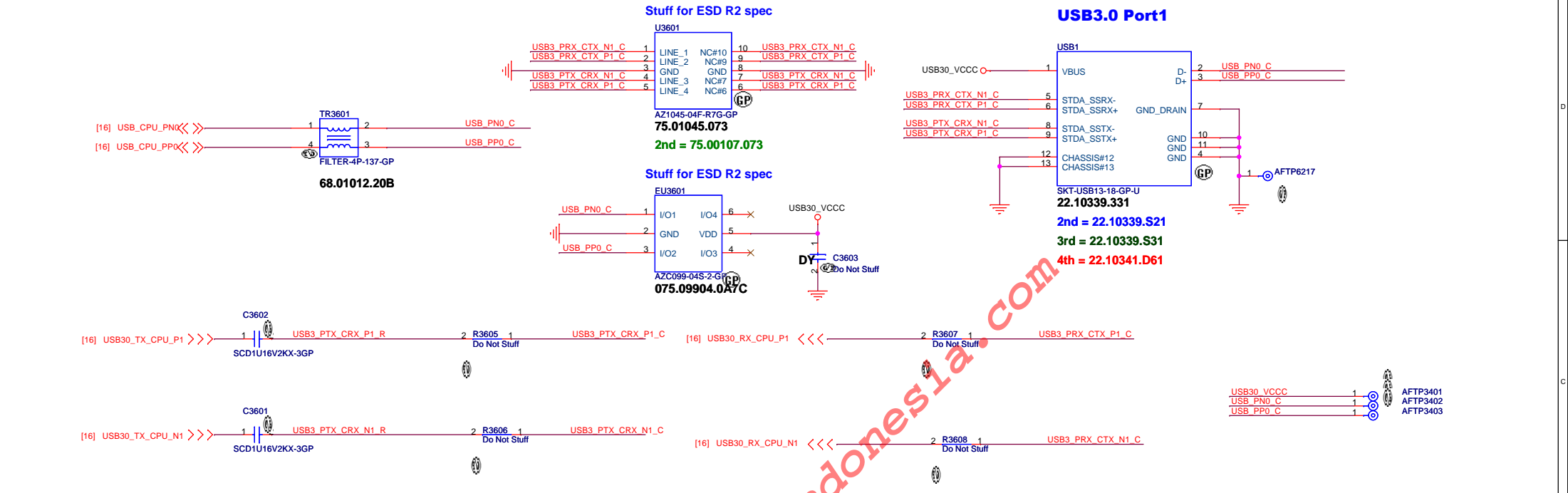
Date: Tuesday, September 15, 2015

Sheet 35 of 105

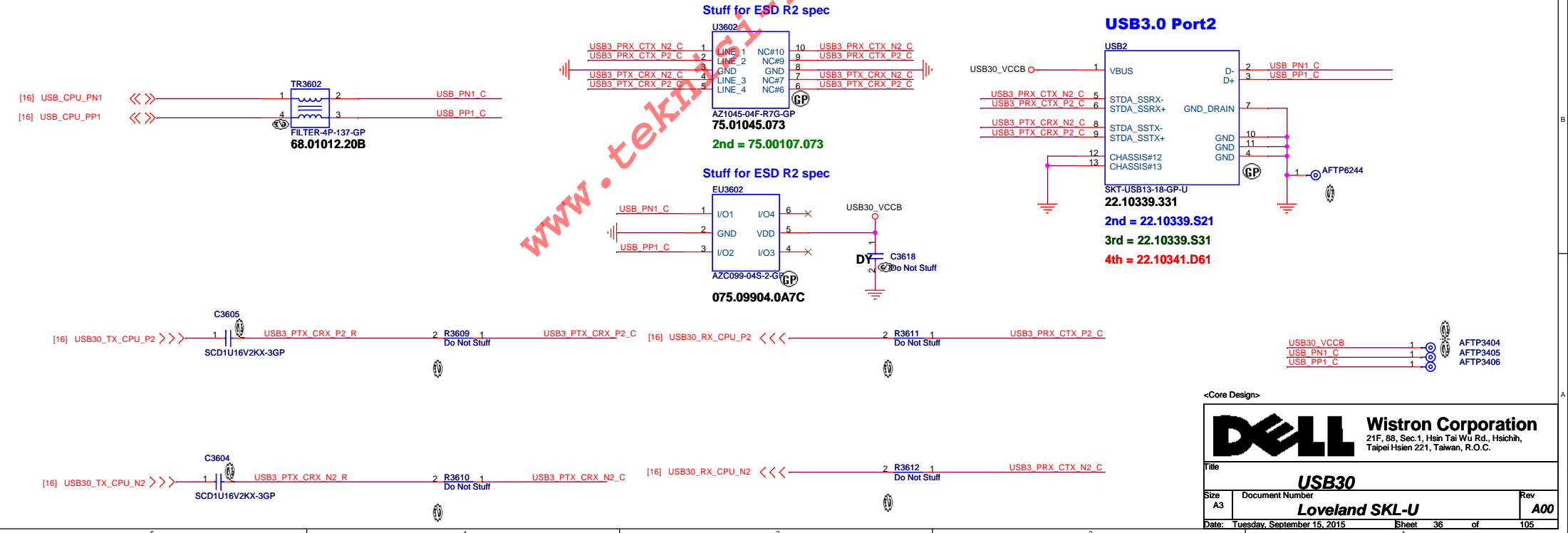
Rev

**A00**

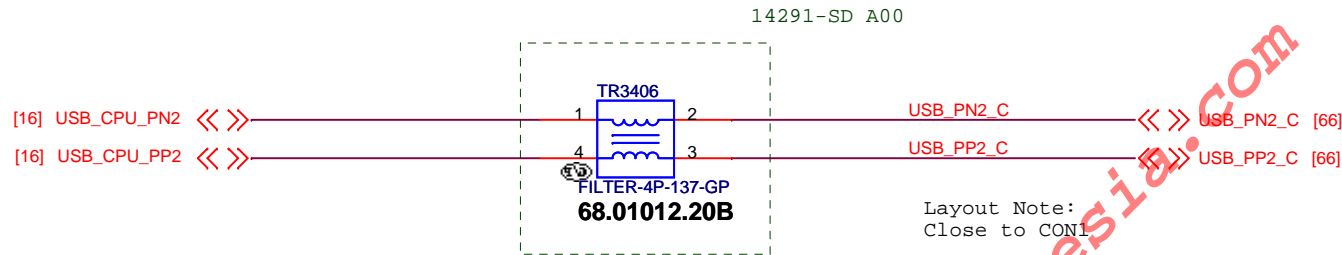
Main Func = USB3.0 Port1



Main Func = USB3.0 Port2

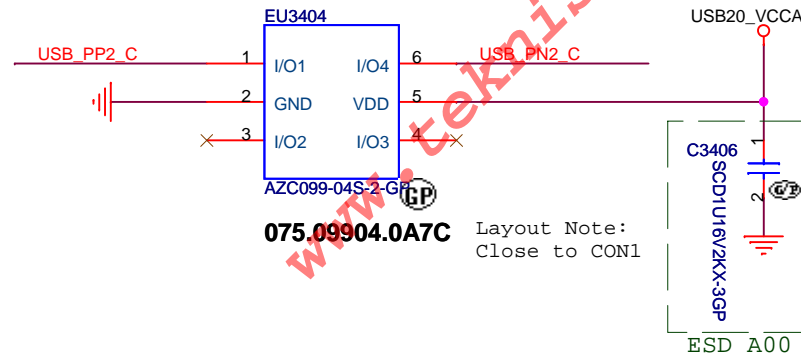


## USB3 (USB2.0) CMC



## USB ESD Diode

Stuff for ESD R2 spec



<Core Design>


<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>USB20</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
Date: Tuesday, September 15, 2015		Sheet 37 of 105	

Main Func = USB3.0 Port1

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<Core Design>


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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
Date: Tuesday, September 15, 2015		Sheet 38 of	105

Main Func = USB3.0 Port1

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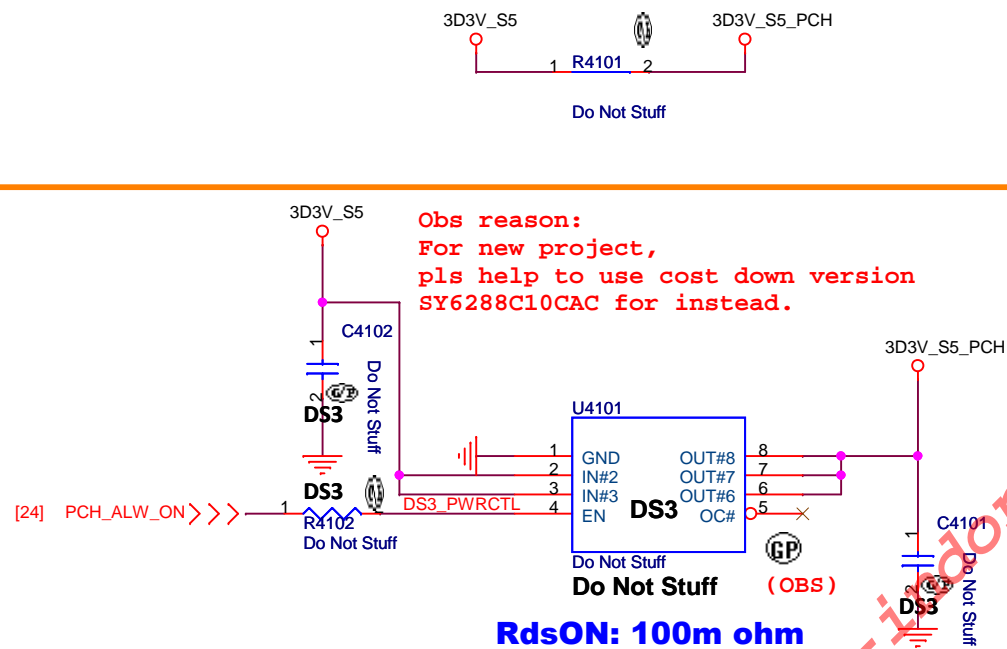
<Core Design>

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
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Main Func = Power Plane & Sequence



DS3

<Core Design>



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Title

**Connected\_Standby(1/2)+DS3**

Size  
A4

Document Number

**Loveland SKL-U**

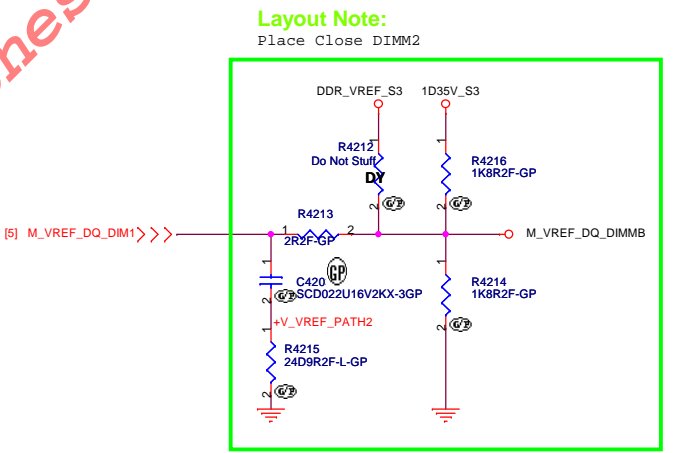
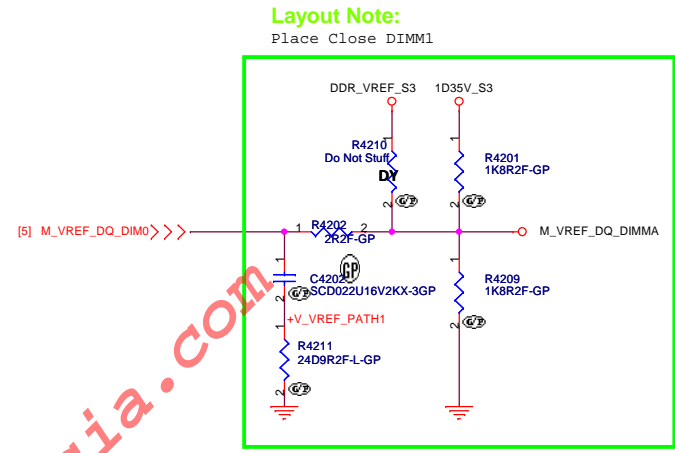
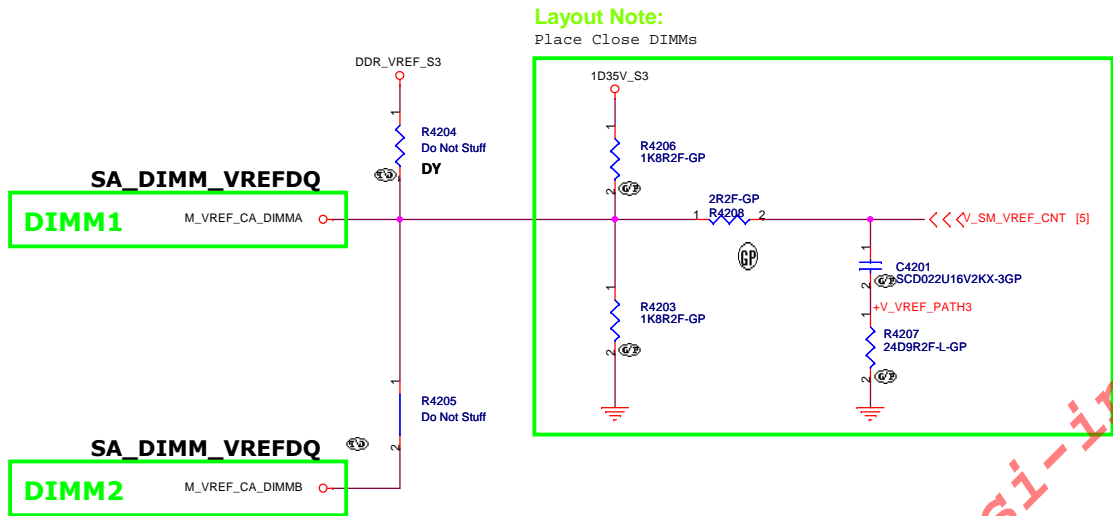
Rev  
**A00**

Date: Tuesday, September 15, 2015

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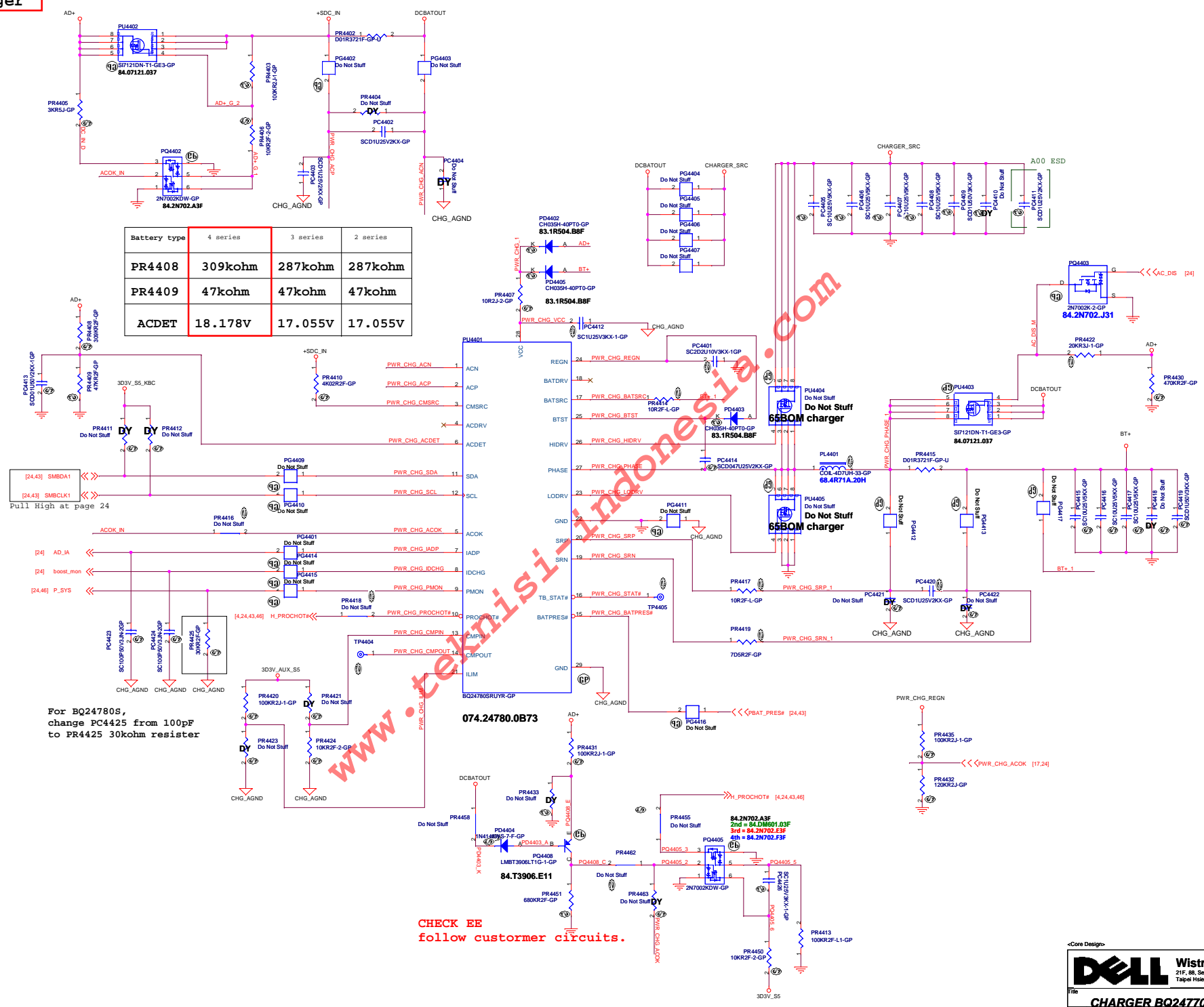
Main Func = DIMM1  
Main Func = DIMM2

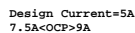
VREF CIRCUITRY





Main Func = Charger

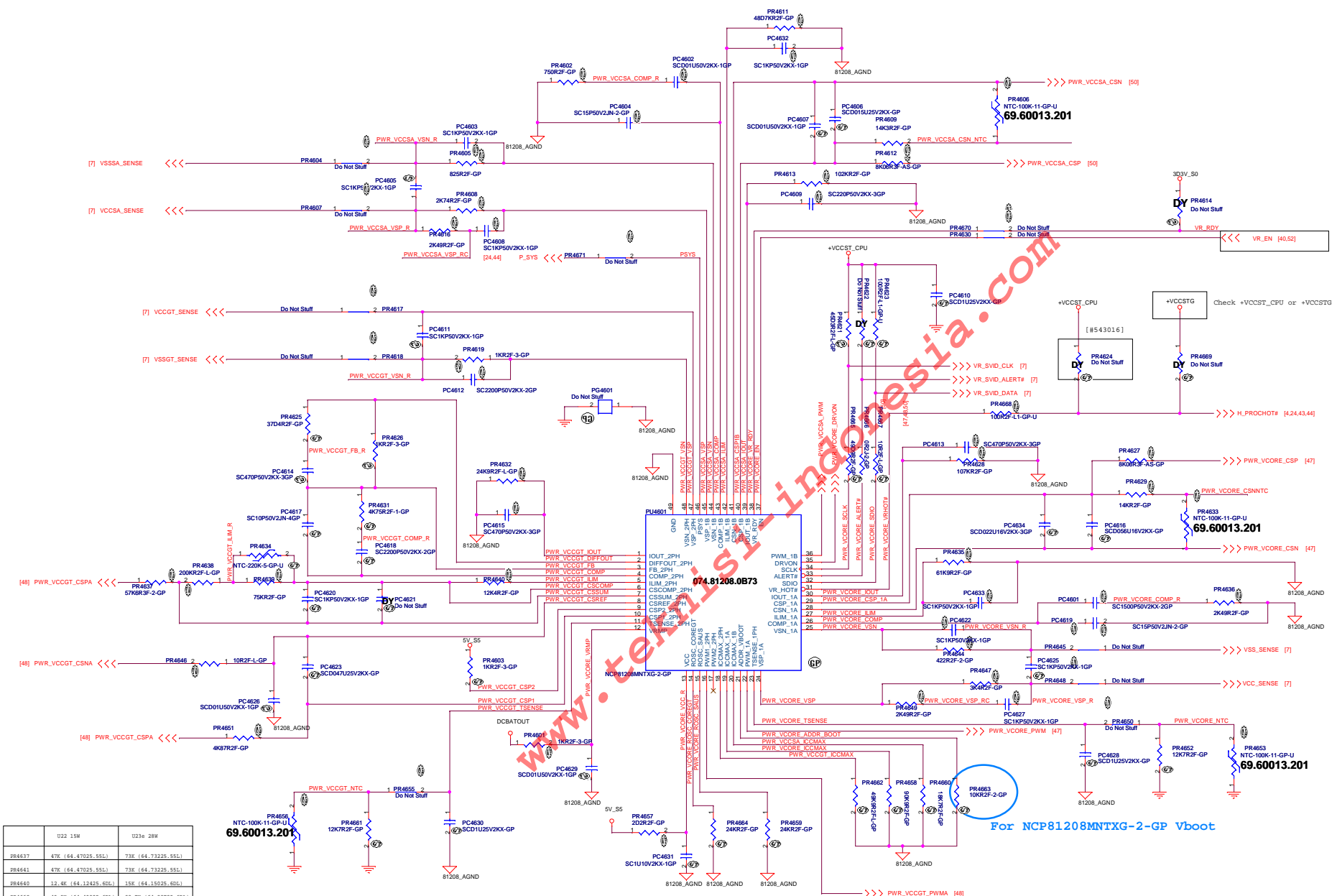




Design Current=7A  
10.5A<OCP>12.6A

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
 Inductor: CHIP CHOKE 2.2U PCMC063T-2R2Mn 18mohm/20mohm Isat =14Arms 68.2R210.20B  
 O/P capCHIP CAP L 220V 6.3V M6.3\*4.4 / Chemi-con/ 18mohm / 79.22710.3KL  
 H/S:IS1412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
 L/S:IS1870 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.13m

	U22 15W	U23a 28W
PR4637	47K (64.47025, 55L)	73K (64.73225, 55L)
PR4641	47K (64.47025, 55L)	73K (64.73225, 55L)
PR4640	12.4K (64.12425, 60L)	15K (64.15025, 60L)
PR4652	49.9K (64.49925, 60L)	89.7K (64.89725, 60L)
PR4658	88.7K (64.88725, 60L)	95.9K (64.90925, 60L)
PR4647	2.37K (64.23715, 60L)	2.15K (64.21515, 60L)
PR4635	38.3K (64.38325, 60L)	37.4K (64.37425, 60L)
PR4628	73.2K (64.73225, 60L)	69.8K (64.69825, 60L)










Main Func = CPU\_CORE

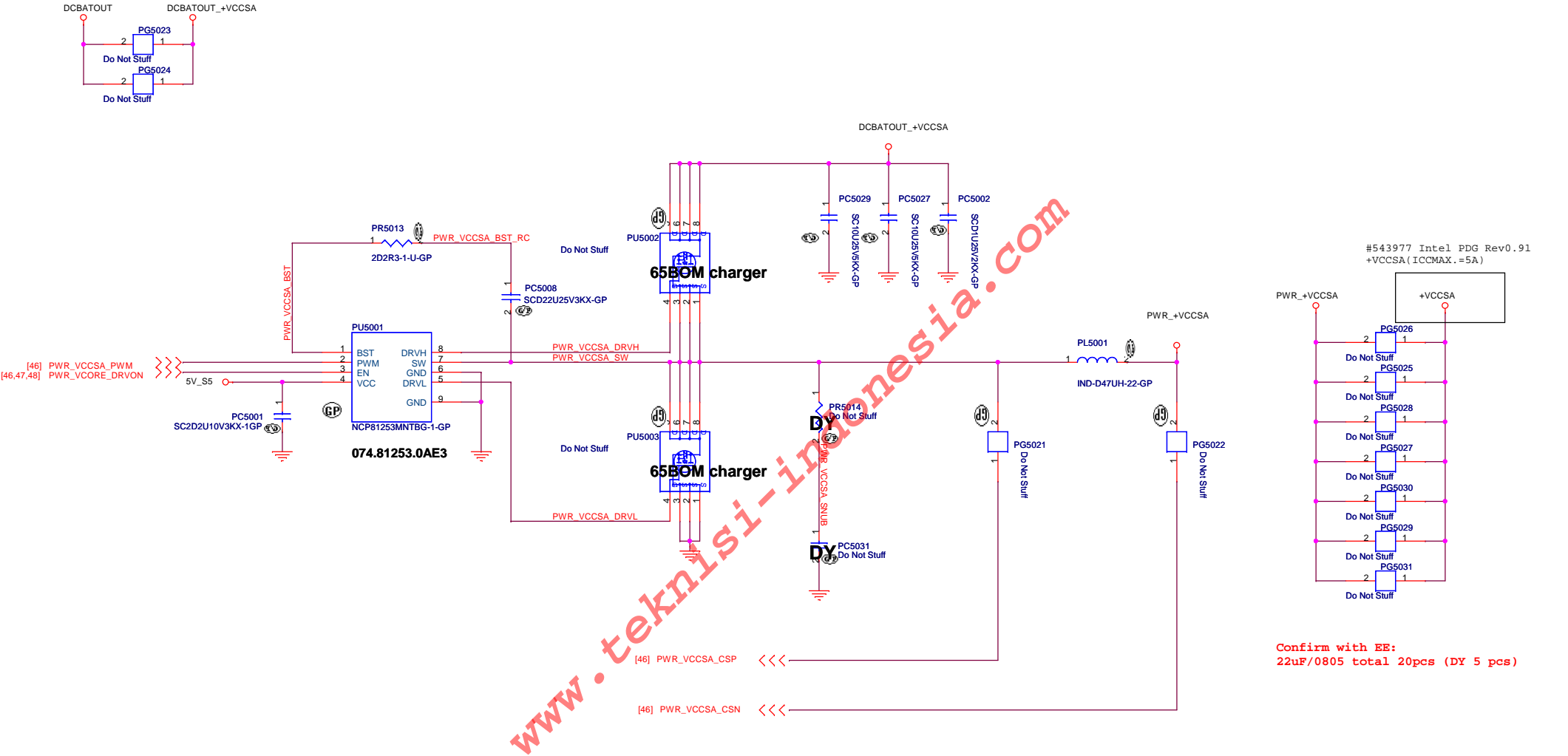
(Blanking)

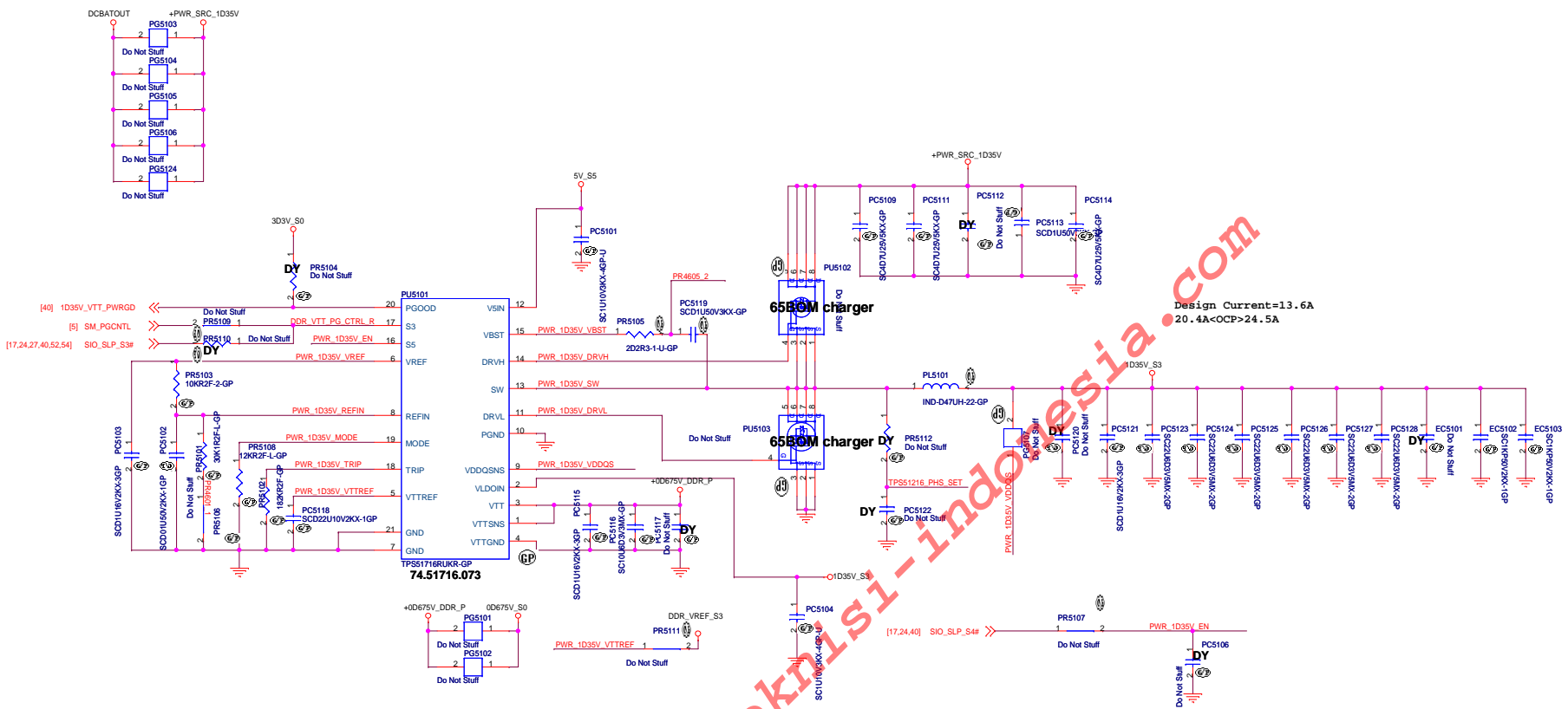
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<Core Design>

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Title <b>NCP81210MN_CPU_VCCGTUS</b>			
Size A4	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
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Main Func = CPU\_CORE

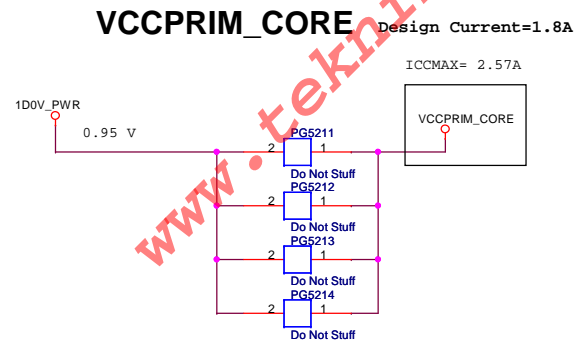
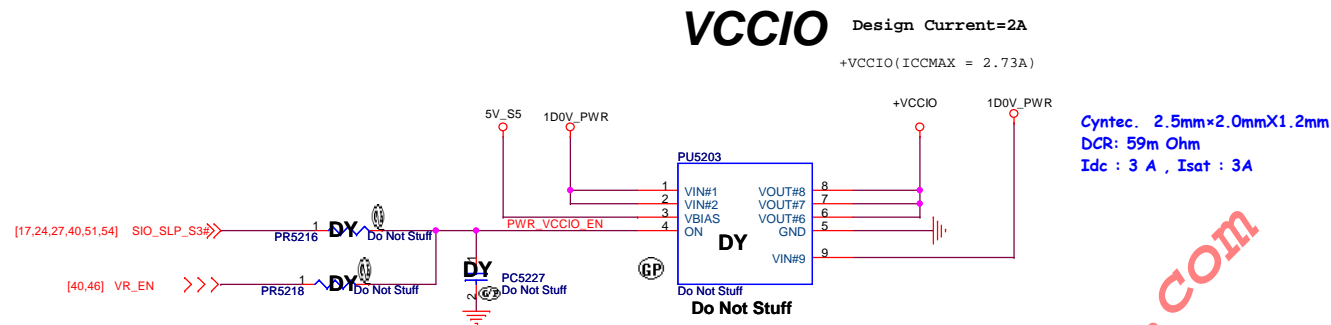





Design Current=13.6A  
20.4A<OCP>24.5A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

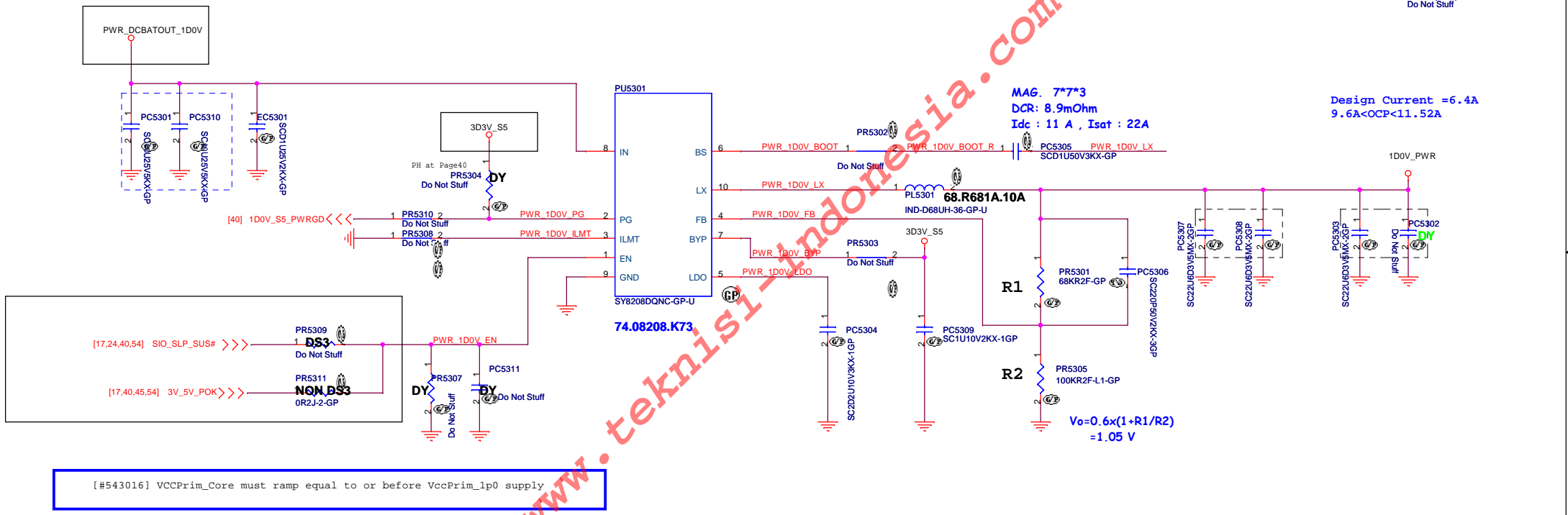
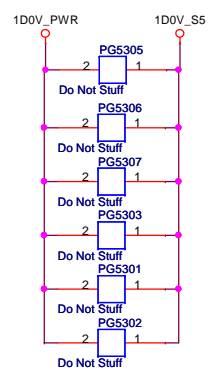
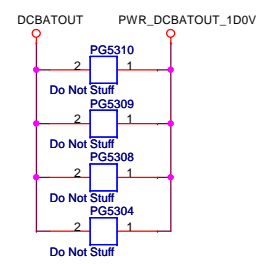
I/P cap: 10U 25V K0805 X5R / 78.10622.51L  
Inductor: CHIP CHOKER 0.68UH PCMC063T-R68 4~4.2mohm Isat =26Arms 68.R4710.10M  
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L  
H/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SI5780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037



<Core Design>

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Title			
<b>DCDC-0D975V_VCCIO</b>			
Size A3	Document Number <b>Loveland SKL-U</b>	Rev <b>A00</b>	
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Main Func = 1D0V



MAG: 7\*7\*3  
DCR: 8.9mOhm  
Idc : 11 A , Isat : 22A

Design Current =6.4A  
9.6A<OCP<11.52A


$$V_o = 0.6 \times (1 + R1/R2) = 1.05 V$$

[17,24,40,54] SIO\_SLP\_SUS# >>>  
[17,40,45,54] 3V\_5V\_POK >>>

[#543016] VCCPrim\_Core must ramp equal to or before VccPrim\_lp0 supply

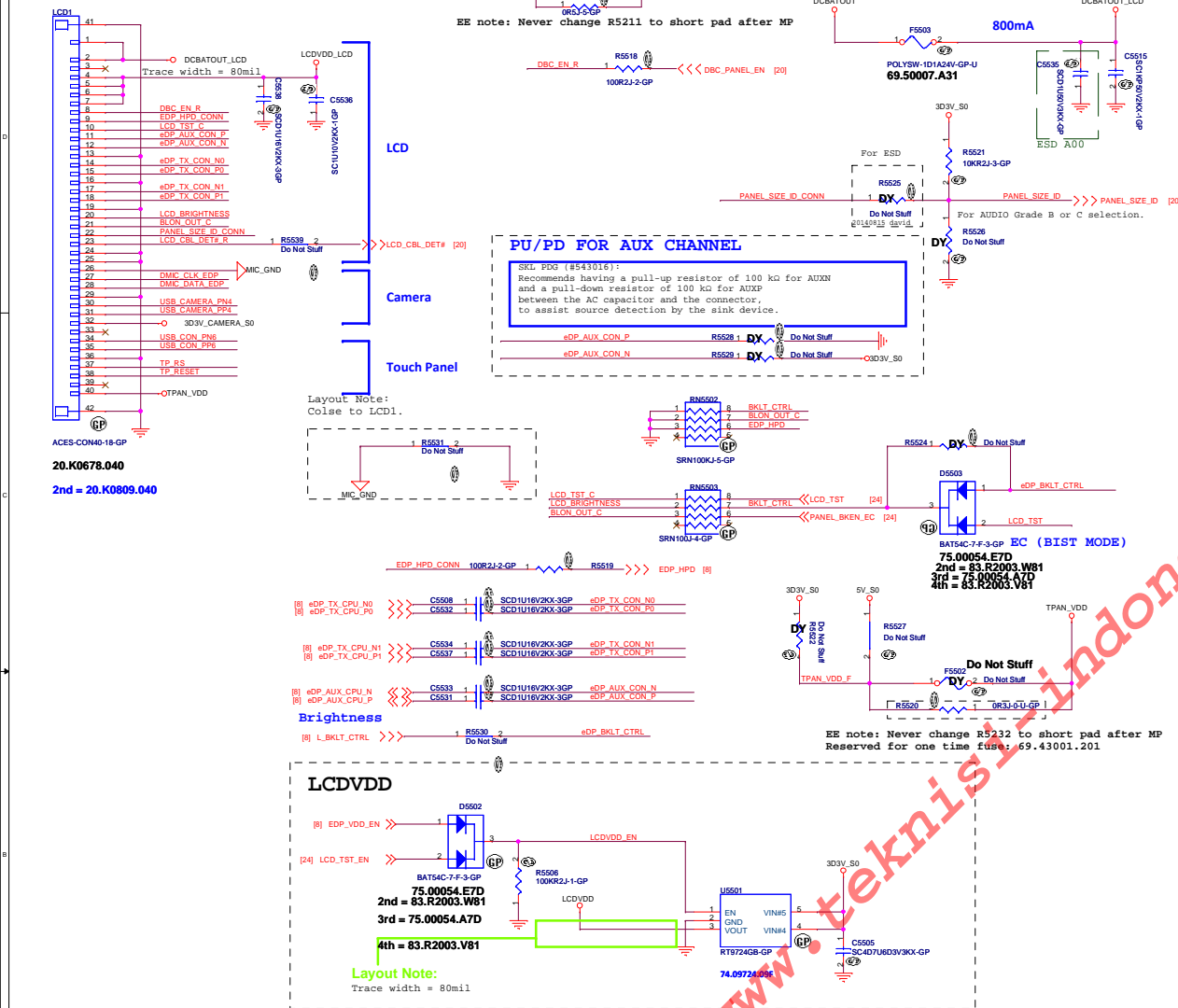
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP EL 330U 2.5V M6.3\*4.4 3.5Arms Chemi-con/ 79.3371V.6CL  
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

<Core Design>

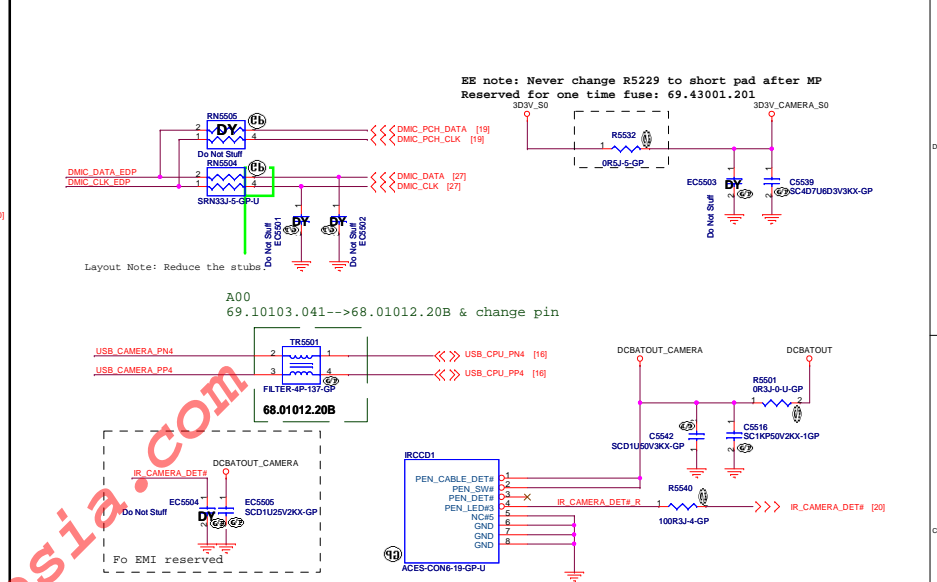
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>DCDC-V1D00A</b>			
Size A3	Document Number <b>Loveland SKL-U</b>		Rev <b>A00</b>
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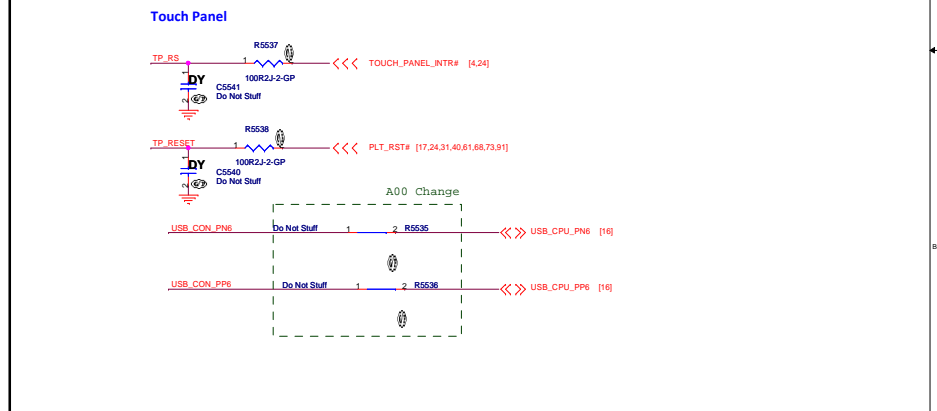
# Main Func = LCD



# Main Func = CAM



# Main Func = TS




«Core Design»

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Title <b>CRT</b>			
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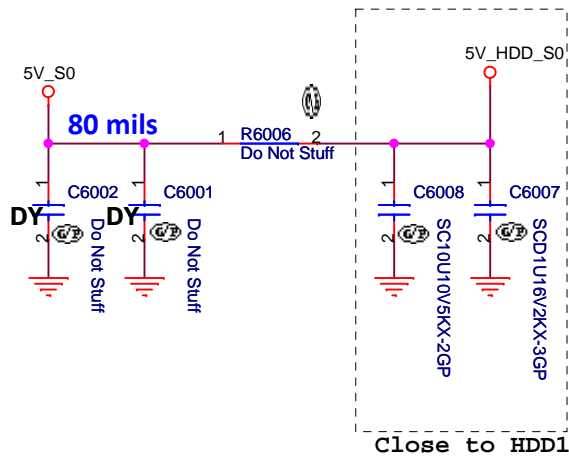
(Blanking)

<Core Design>

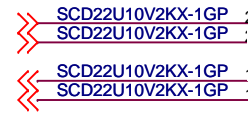
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
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Main Func = HDD

# SATA HDD Connector



[16] SATA\_TX\_CPU\_P0  
[16] SATA\_TX\_CPU\_N0  
[16] SATA\_RX\_CPU\_N0  
[16] SATA\_RX\_CPU\_P0



[20] HDD\_DET# <<<  
Do Not Stuff

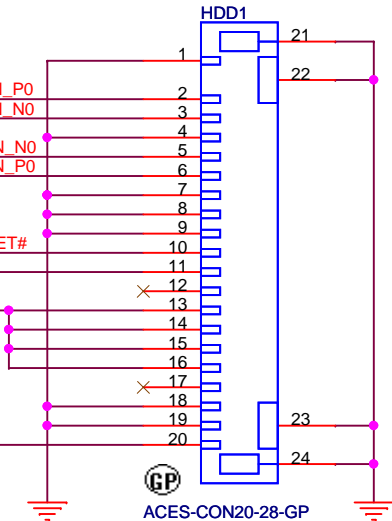


[67] FFS\_INT2\_Q >>>

5V\_HDD\_S0

[67] HDD\_DEVSLEP >>>  
Do Not Stuff

HDD\_DEVSLEP\_R



20.F2036.020

5V\_HDD\_S0 1 AFTP5601 Do Not Stuff

3D3V\_AUX\_S5

R6003 Do Not Stuff

5V\_HDD\_ENABLE#

DCBATOUT

R6002 Do Not Stuff

5V\_S0

5V\_HDD\_S0

Q6001 Do Not Stuff  
Do Not Stuff  
2nd = 084.27002.003F  
3rd = 84.2N702.E3F

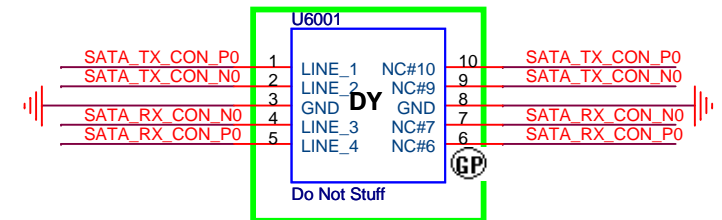
R6004 Do Not Stuff

HDD\_PWR\_EN\_R

R6005 Do Not Stuff

U6002 Do Not Stuff  
Do Not Stuff  
2ND = 84.P2703.03D  
3rd = 84.03456.D3D  
AO6402A MAX 7A  
Rds(on) = 27~40m Ohm

C6009 Do Not Stuff



Do Not Stuff  
Layout Note:  
Place near HDD1

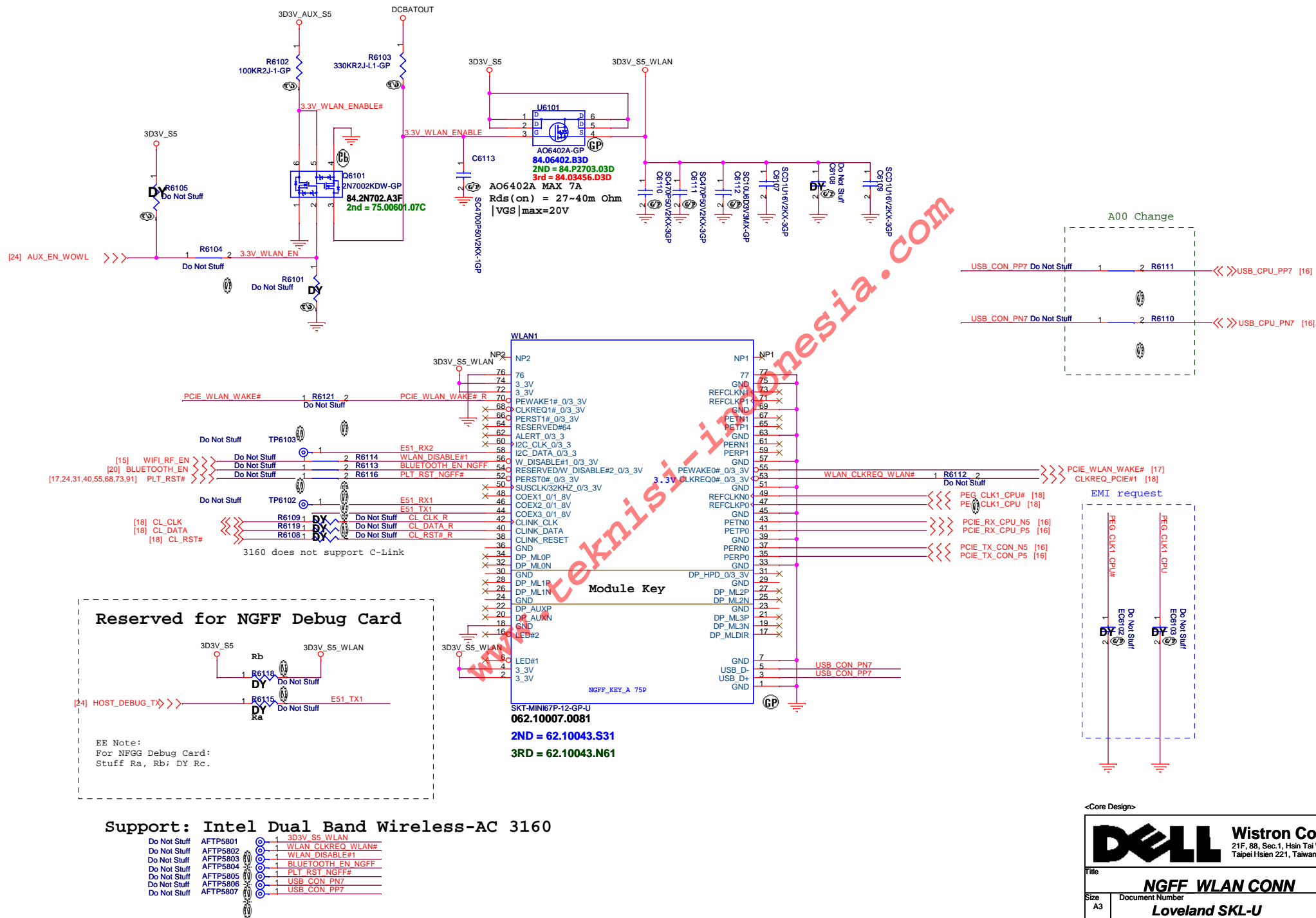
<Core Design>



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Title			SATA HDD	
Size	Document Number		Rev	
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## Main Func = WLAN



&lt;Core Design&gt;



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Title

**NGFF WLAN CONN**

Size

Document Number

**Loveland SKL-U**

Date \_\_\_\_\_

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Date \_\_\_\_\_

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<b>Reserved</b>			
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Title (Reserved)

Size A4	Document Number <b>Loveland SKL-U</b>	Rev <b>A00</b>
------------	--	-------------------

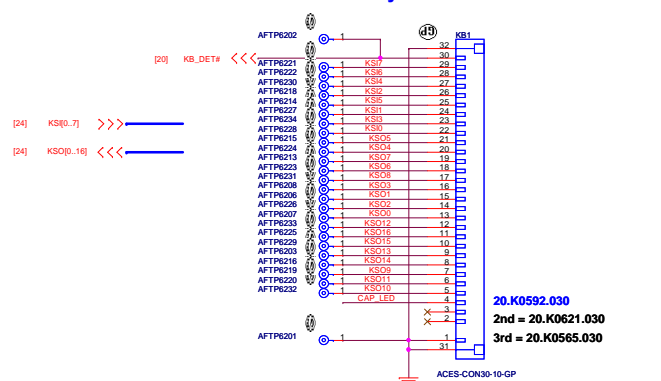
Date: Tuesday, September 15, 2015 Sheet 63 of 105



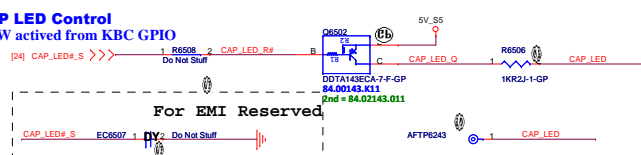


Main Func = KB					Main Func = TPAD				
----------------	--	--	--	--	------------------	--	--	--	--

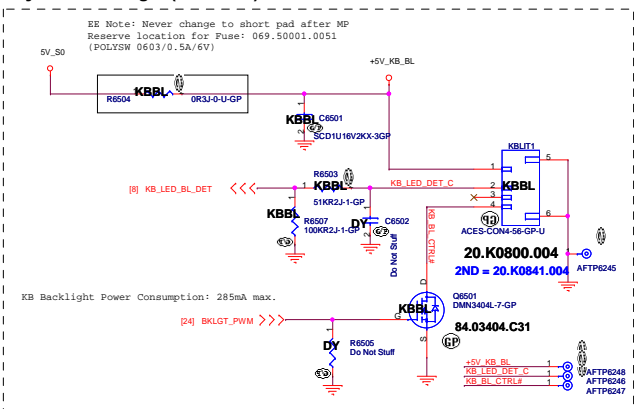
### Internal Keyboard Connector



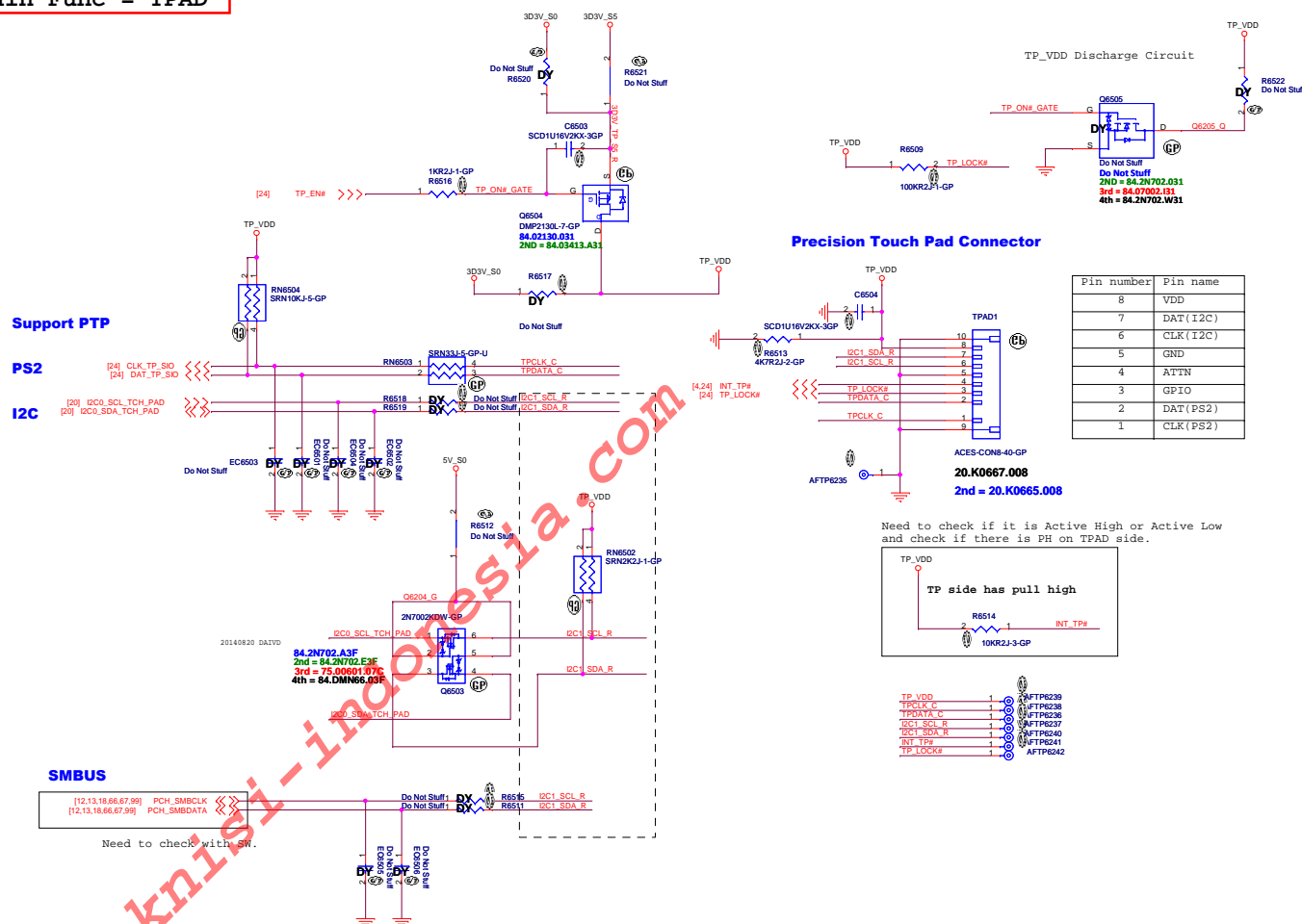
**CAP LED Control**  
LOW activated from KBC GPIO



**Keyboard Backlight (Reserved)**



Main Func = TPAD



Pin number	Pin name
8	VDD
7	DAT(I2C)
6	CLK(I2C)
5	GND
4	ATTN
3	GPIO
2	DAT(PS2)
1	CLK(PS2)

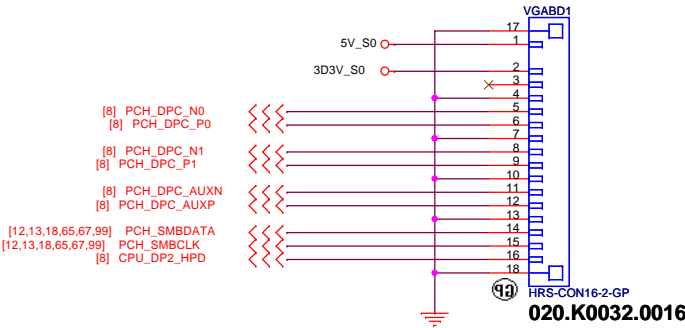
Need to check if it is Active High or Active Low  
and check if there is PH on TPAD side.

[illegible]

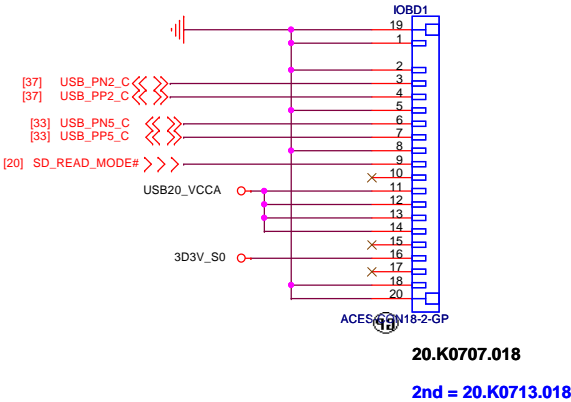
TP_VDD	1	①	AFTP6239
TPCLK_C	1	②	AFTP6238
TPDATA_C	1	③	AFTP6236
I2C1_SCL_R	1	④	AFTP6237
I2C1_SDA_R	1	⑤	AFTP6240
INT_TP#	1	⑥	AFTP6241
TP_LOCK#	1	⑦	AFTP6242

Main Func = IO Connector

VGA Connector



I/O Board Connector

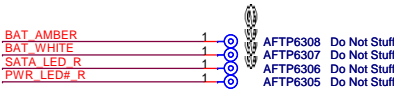
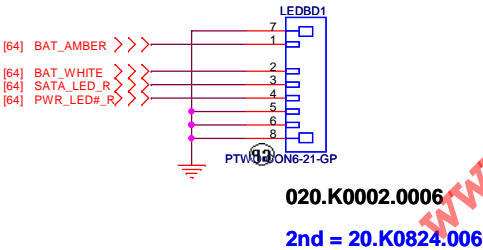


Pitch: 1mm

Power: 5 pins

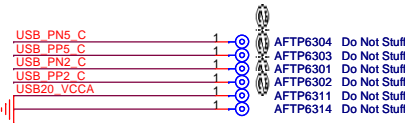
GND: 5 pins

LED Connector



USB3 (USB2.0)

Cardreader (USB2.0)








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Main Func = Hall Sensor

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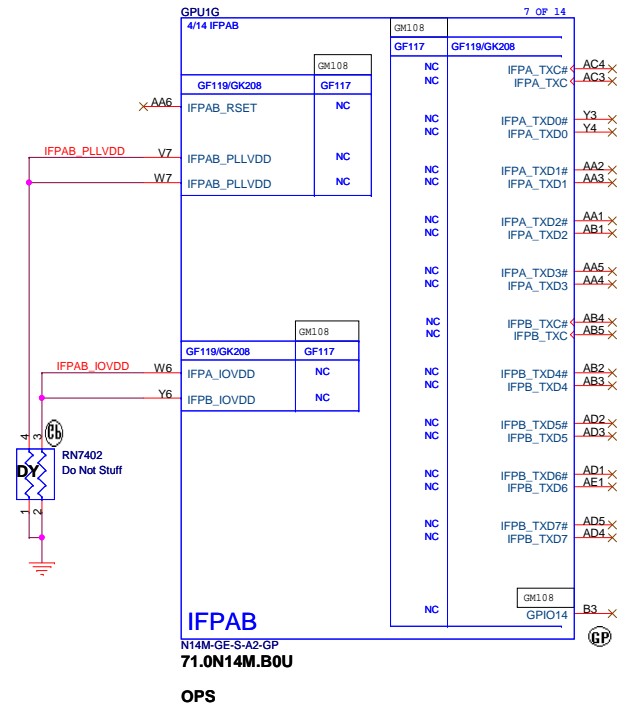
<Core Design>

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Title		
<b>USB3.0 PORT</b>		
Size A4	Document Number <b>Loveland SKL-U</b>	Rev <b>A00</b>
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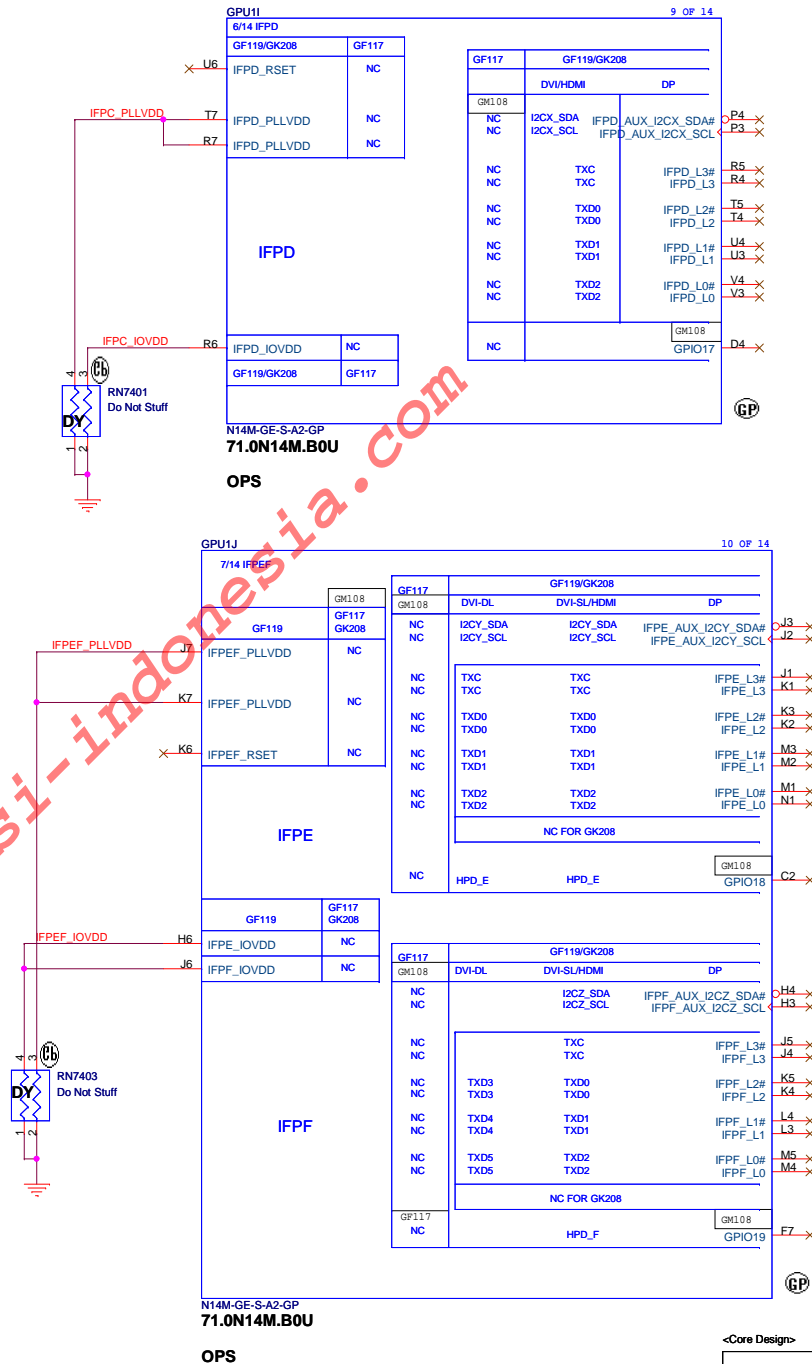
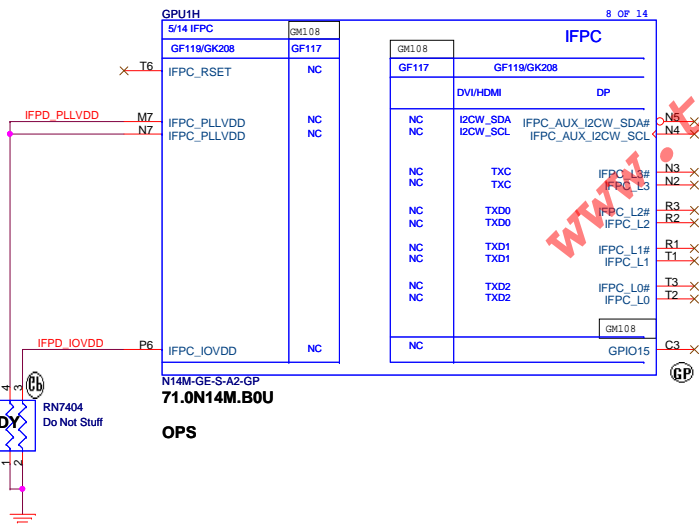




## LVDS Interface



## HDMI Interface



&lt;Core Design&gt;



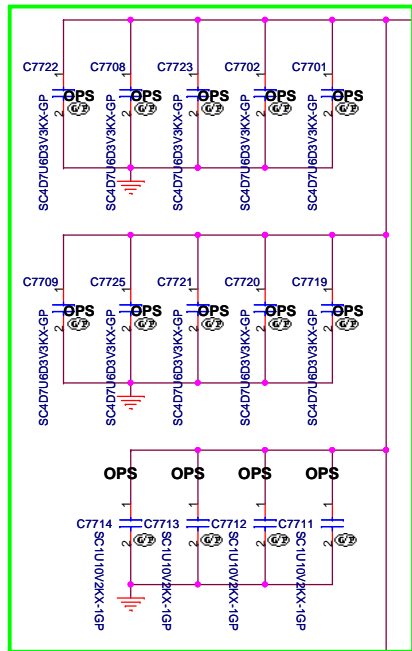
Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.



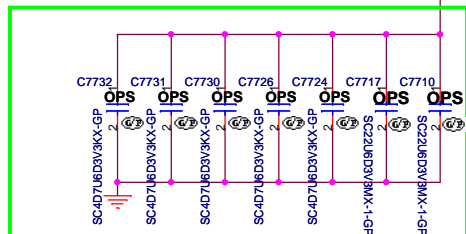


# Main Func = dGPU

## Under GPU



## Near GPU



VGA\_CORE

GPU1E 5 OF 14

71.0N14M.B0U

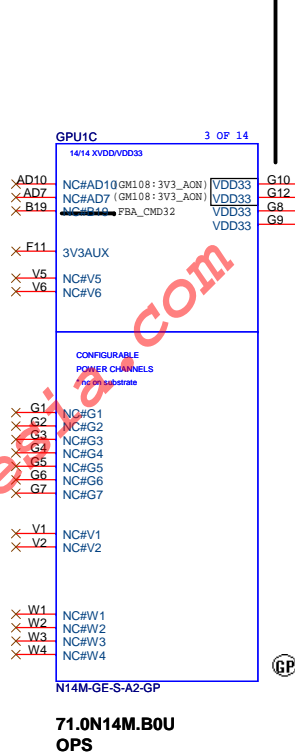
OPS

GPU1F 6 OF 14

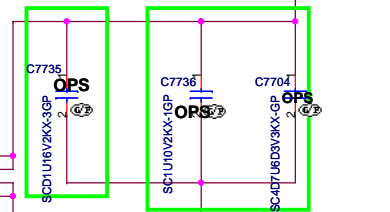
71.0N14M.B0U

OPS

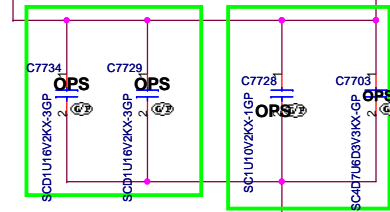
G10,G12:  
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.  
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



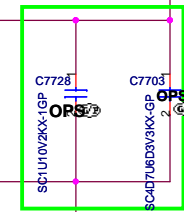
## Under GPUNear GPU



## Under GPU



## Near GPU



3.3V +/- 5%  
85mA

Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S	0402	2
GB4B-128		1 µF	X5R	0603	1
GB3-256		4.7 µF	X5R	0603	1
GB2B-64	3V3_AON	0.1µF	X6S	0402	1
GB4B-128		1 µF	X5R	0603	1
GB3-256		4.7 µF	X5R	0603	1

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

Table 3-6. NVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	Under GPU
	1 µF	X6S	0402	4	Under GPU
	47 µF	X5R	0805	1	Near GPU
	22 µF	X5R	0805	1	Near GPU
	4.7 µF	X5R	0805	5	Near GPU
	330 µF	POS	7343	1	Near GPU

ESR ≤ 6 mΩ

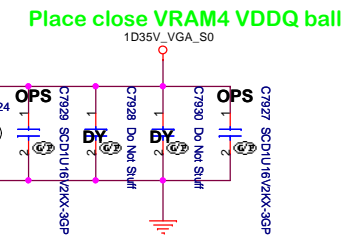
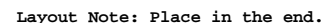
<Core Design>

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Title: **GPU(5/5)PWR/GND**  
Size: A3 Document Number: **Loveland SKL-U** Rev: **A00**  
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Title		
<b>GPU-VRAM5,6 (3/4)</b>		
Size A4	Document Number <b>Loveland SKL-U</b>	Rev <b>A00</b>
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Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number		Rev
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N16V\_GM\_B1  
Config B

Design Current=33.5A  
56.65A <OCP> 66.7A

Component Value	N15V-QM-B Config D	N16V-QM-B1 Config B
R1 (PR8222)	27K 64.27025, 60L	20K 64.20025, 60L
R2 (PR8206)	7.5K 64.75015, 60L	20K 64.20025, 60L
R3 (PR8208)	0 63.80014, 10L	2K 64.20015, 60L
R4+R5 (PR8209)	7.5K 64.75015, 60L	1.8K 64.18025, 60L
C (PC8233)	5.60F 78.56222, 28F	2.70F 78.27224, 28F

78.56222, 28F <OBS REASON> 50V is more popular, change to 78.56224, 28F

For tuning VGA\_CORE sequence.

I/P cap: 10U 25V K0805 X5R/ 78.10622, 51L  
Inductor: CHIP CHOKER 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms / 68.R2210, 10C  
O/P cap: CHIP CAP EL 330U 2.5V M6.3\*4.4 Chemi-con/79.3371V, 6CL  
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP, 037  
L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06, 037

N16V\_GM\_B1  
Config B

Table 1. PWM-VID Spec and Component Values

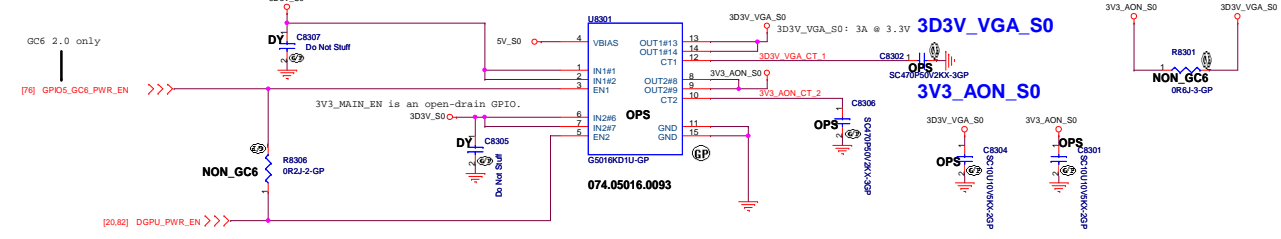
PWM-VID Specification		Config A	Config B
Vmin	V	0.6	0.6
Vmax	V	1.2	1.2
Vboot	V	0.875	0.9
Voltage Step Vstep	mV	6.25	6.25
Number of Voltage Levels N	level	96	96
PWM Frequency F <sub>PWM</sub>	Hz	1.125	1.125
PWM Minimum Pulse Width T <sub>min</sub>	ns	9.26	9.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KQ	39	20
R2 (1%)	KQ	39	20
R3 (1%)	KQ	1.5	2
R4 (1%)	KQ	30	18
R5 (1%)	KQ	1.5	0
C	nF	1.5	2.7

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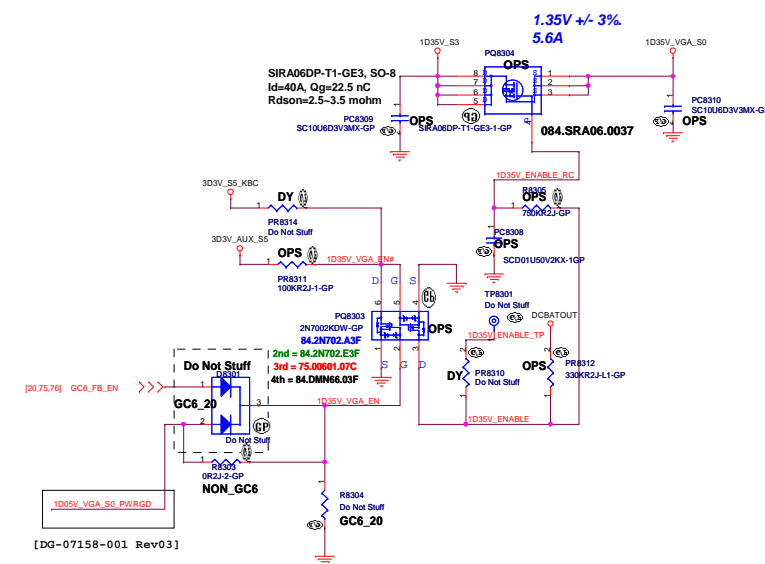
Main Func = dGPU

[DG-07158-001 Rev03] Power up sequence:  
3.3V ==> NVVDD (VGA\_CORE) ==> PEX\_VDD (1.05V) ==> FBVDD/Q (1.35V)

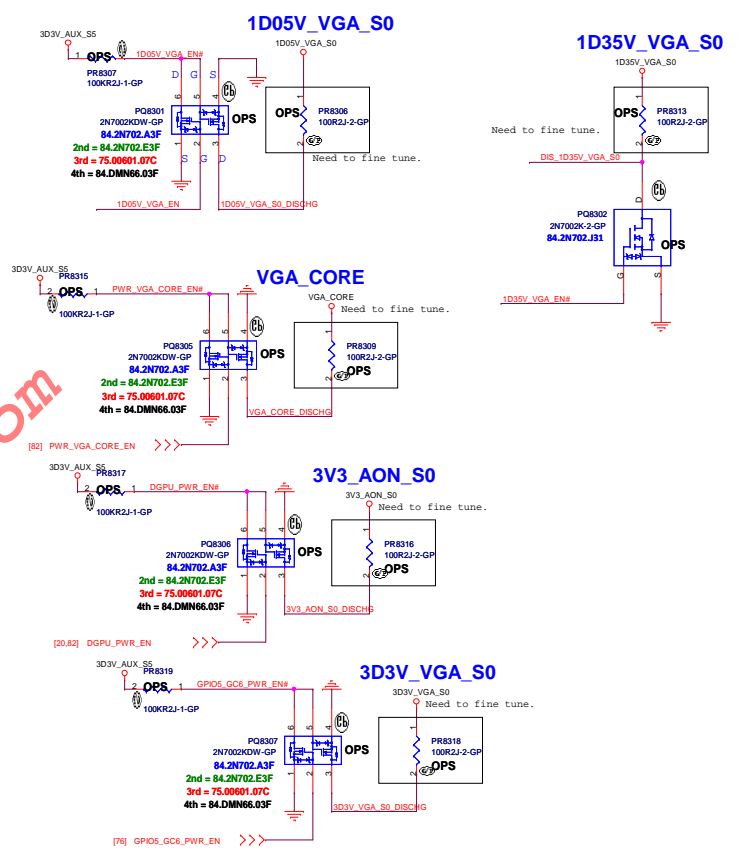
3D3V\_S0 to 3V3\_AON\_S0 and 3D3V\_VGA\_S0



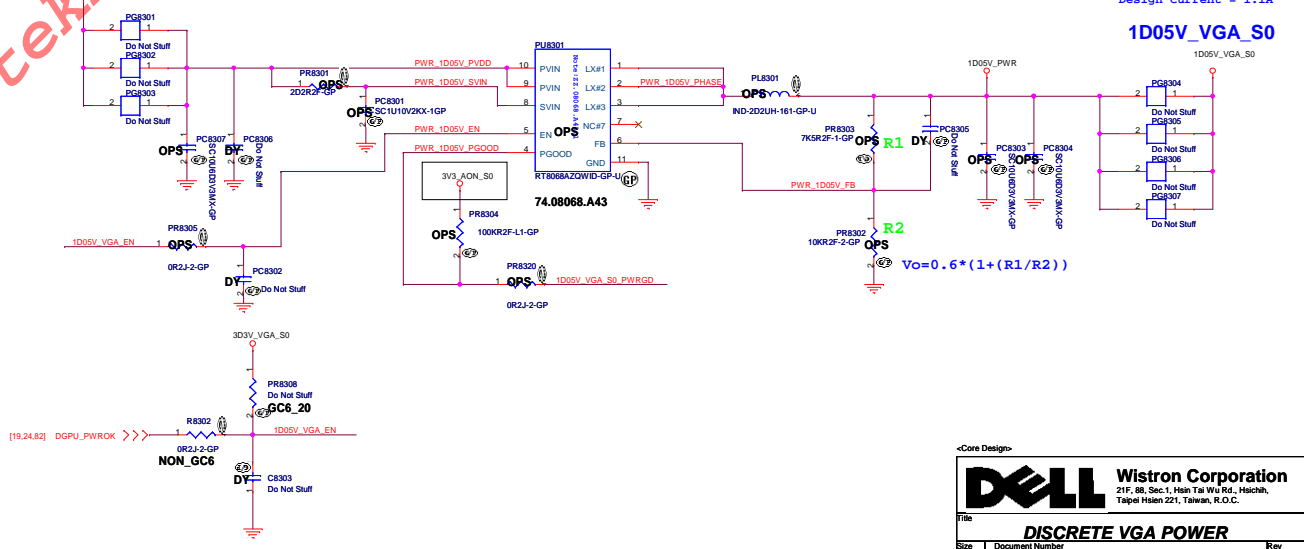
1D35V\_VGA\_S0



dGPU Power Discharge Circuit



RT8068A for 1D05\_VGA



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Title <b>UNUSED PARTS/EMI Capacitors</b>			
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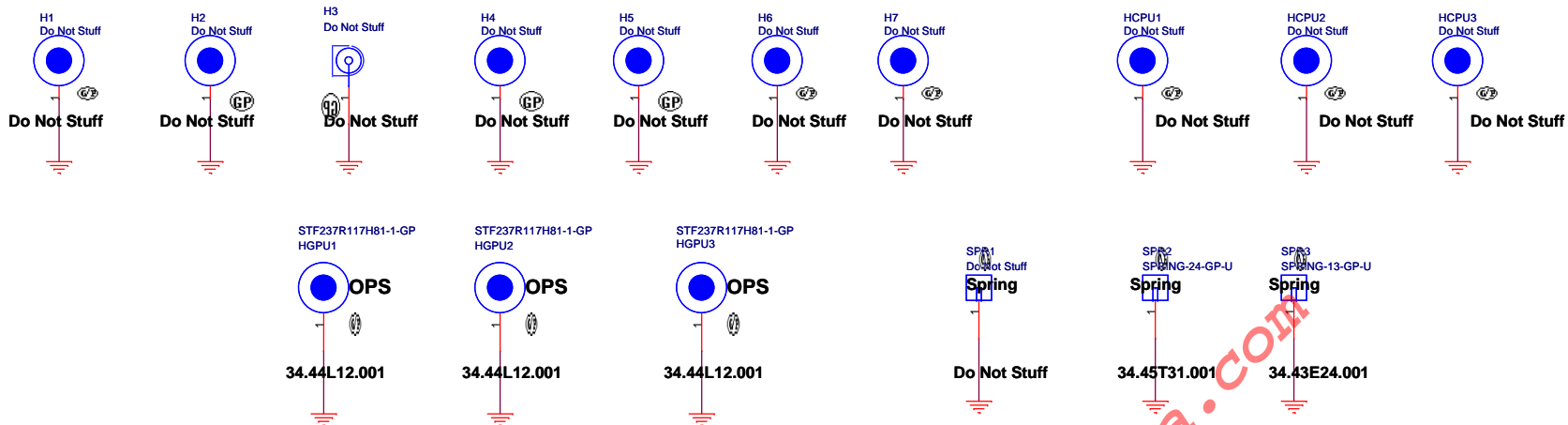
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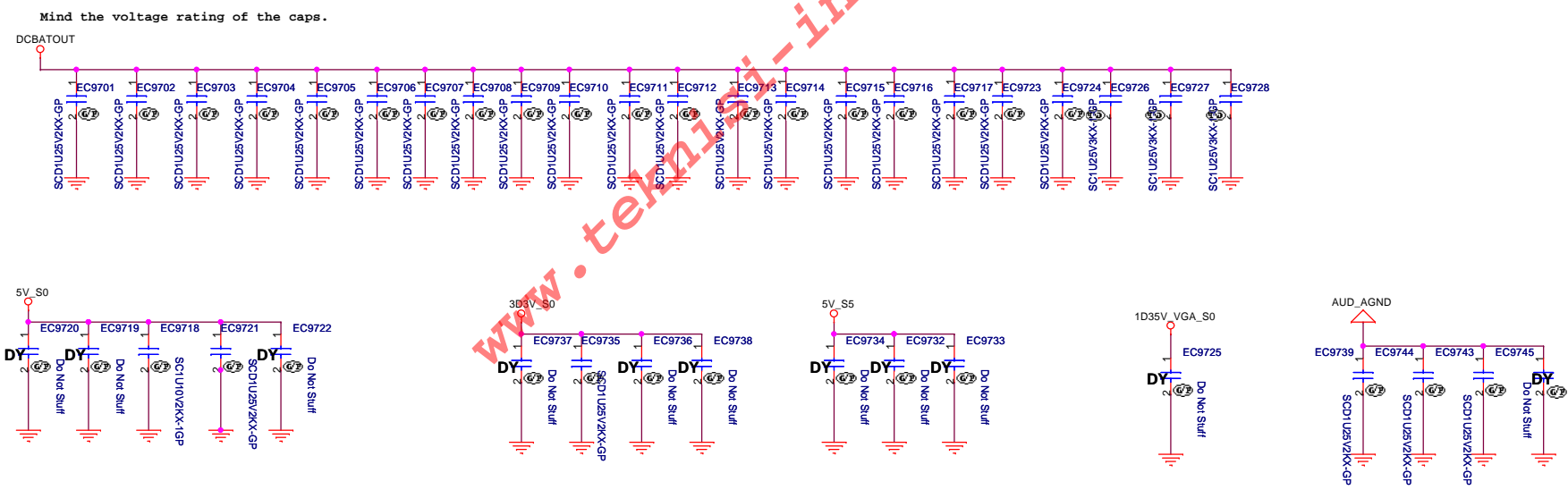
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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<b>Reserved</b>			
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Main Func = UnusedParts



Main Func = EMICapacitors



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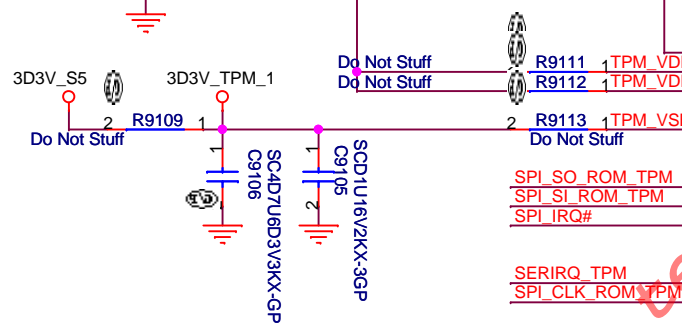
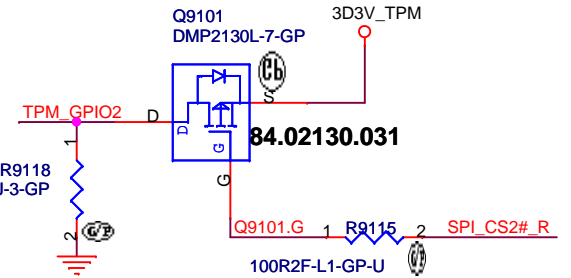
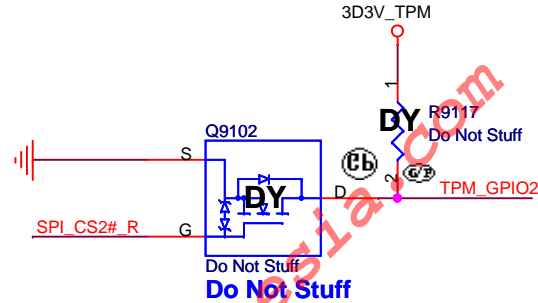
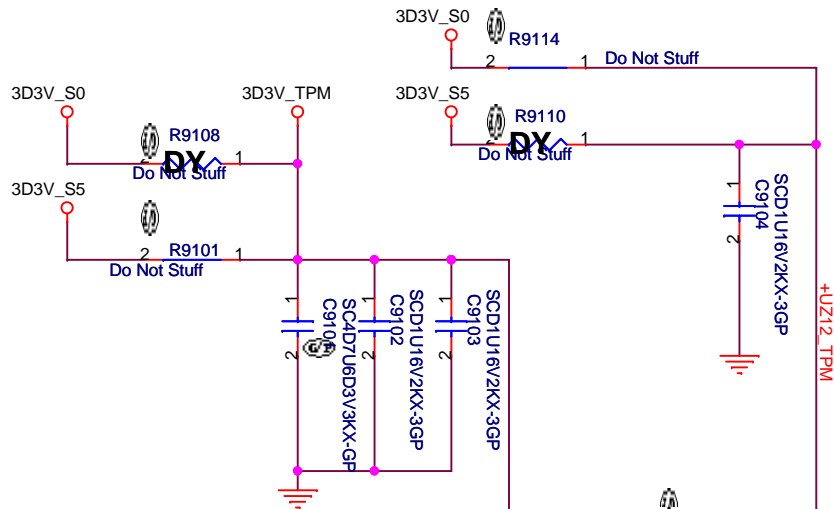
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# SSID = TPM

[18,24,25] SPI\_CLK\_ROM >>> 33R2J-2-GP 1 R9107 SPI\_CLK\_ROM\_TPM  
 [18,24,25] SPI\_SO\_ROM <<< 33R2J-2-GP 1 R9106 SPI\_SO\_ROM\_TPM  
 [18,24,25] SPI\_SI\_ROM >>> 33R2J-2-GP 1 R9105 SPI\_SI\_ROM\_TPM

3D3V\_TPM Do Not Stuff 2 DY R9104 SPI\_IRQ#  
 3D3V\_TPM 10KR2J-3-GP R9103 1 SPI\_CS2#\_R

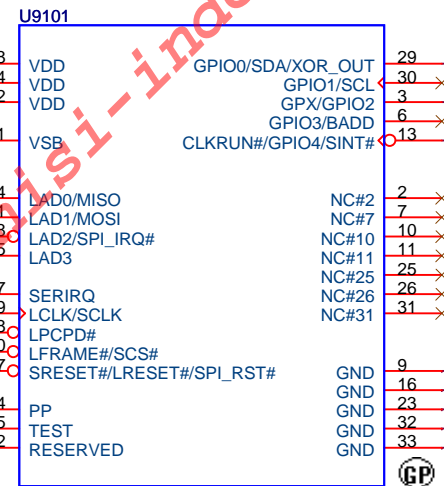
10KR2J-3-GP 2 R9102 1 SERIRQ\_TPM



SPI\_SO\_ROM\_TPM 24 LAD0/MISO NC#2  
 SPI\_SI\_ROM\_TPM 24 LAD1/MOSI NC#7  
 SPI\_IRQ# 15 LAD2/SPI\_IRQ# NC#10  
 LAD3 NC#11  
 NC#25  
 NC#26  
 NC#31

SERIRQ\_TPM 27 SERIRQ  
 SPI\_CLK\_ROM\_TPM 19 LCLK/SCLK  
 LCPD# 28  
 LFRAME#/SCS# 20  
 SRESET#/LRESET#/SPI\_RST# 17

PP 4  
 TEST 5  
 RESERVED 12



NPCT650JAAAYX-GP

071.00650.0A03

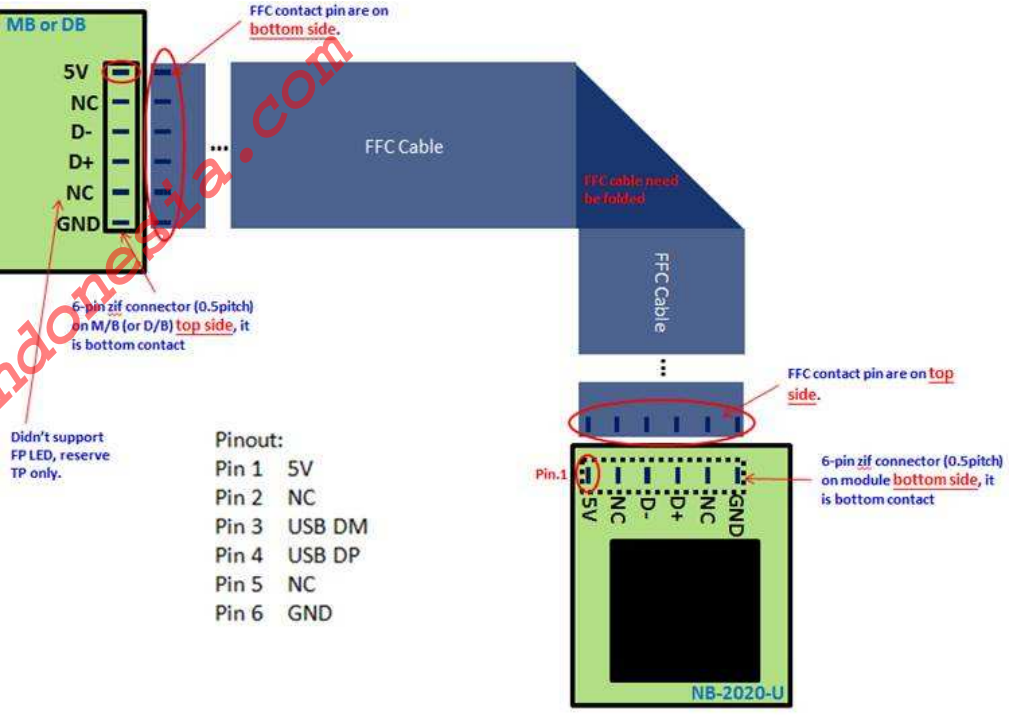
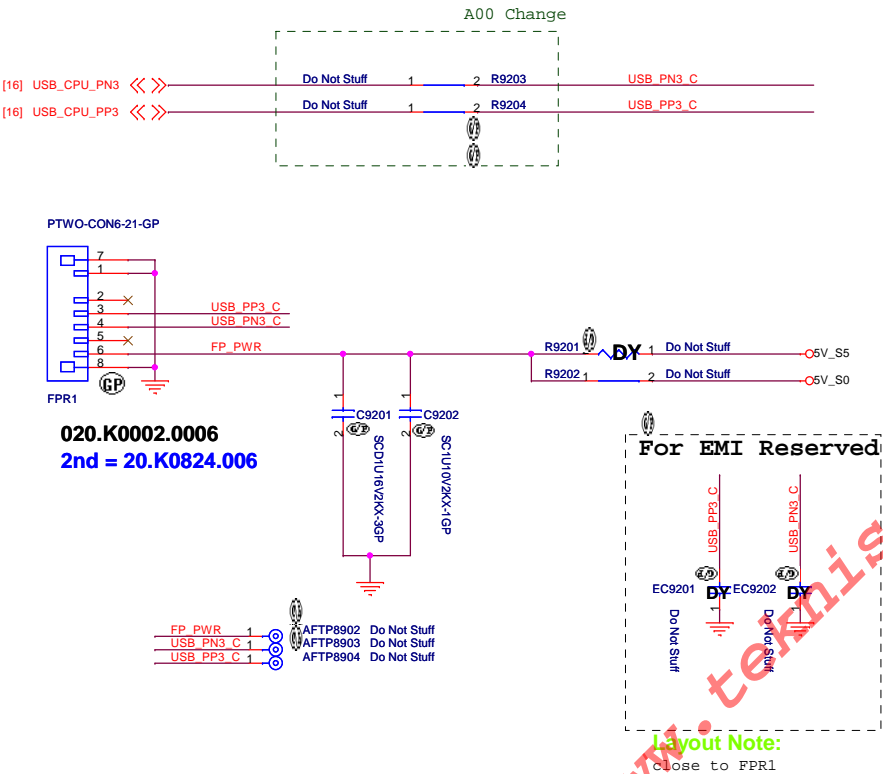
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SSID = Finger Print



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**LVDS\_Switch**

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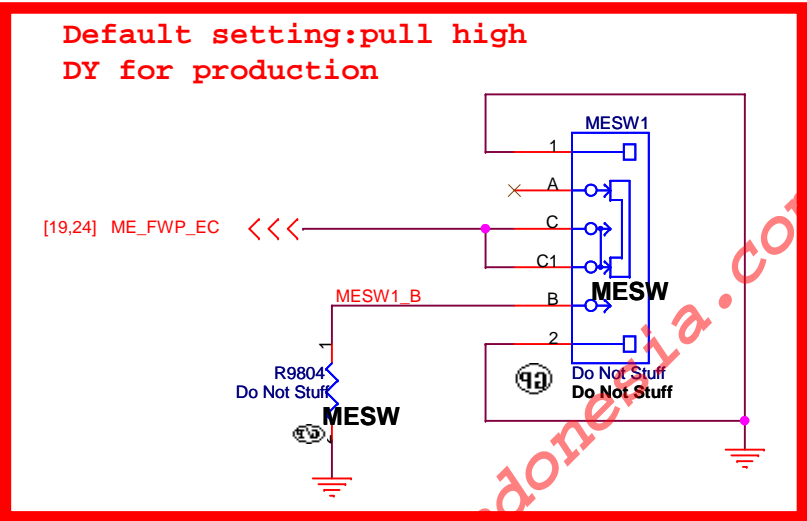
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Firmware SW

Default setting:pull high  
DY for production



	A	B
ME_FWP_SOC	High	Low
	Normal Operation (Default)	Override

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Title

**Firmware SW**

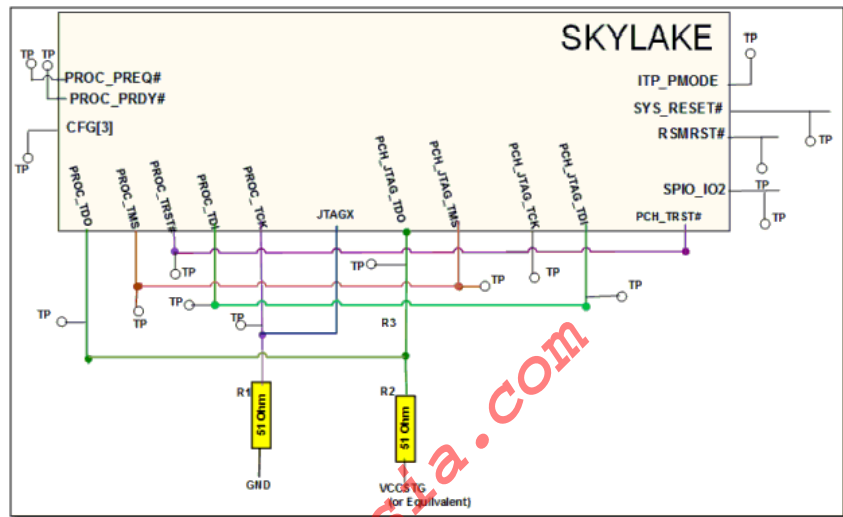
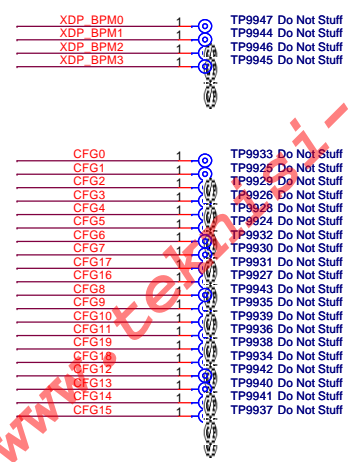
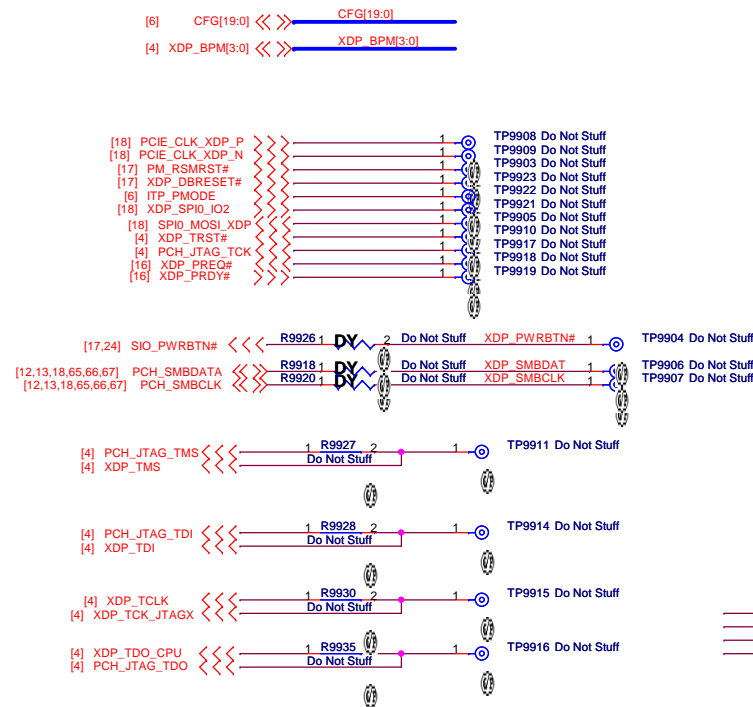
Size  
A4

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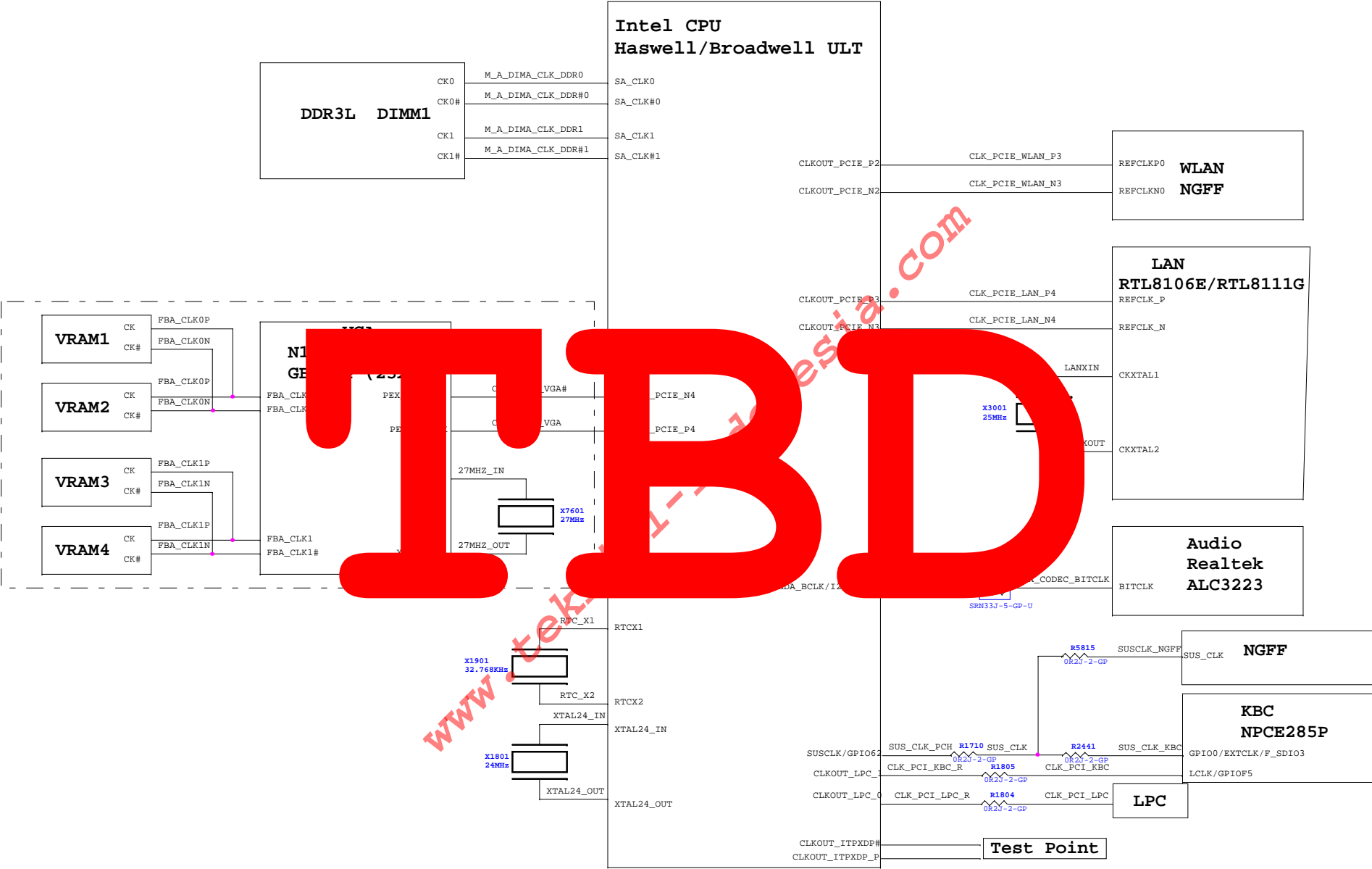
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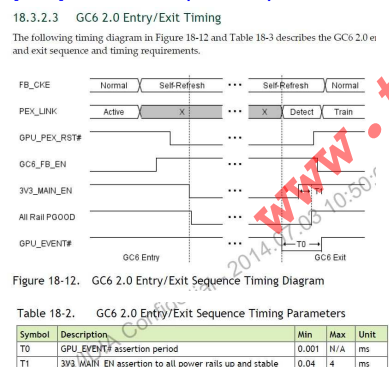
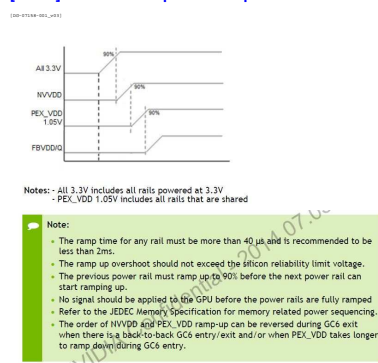
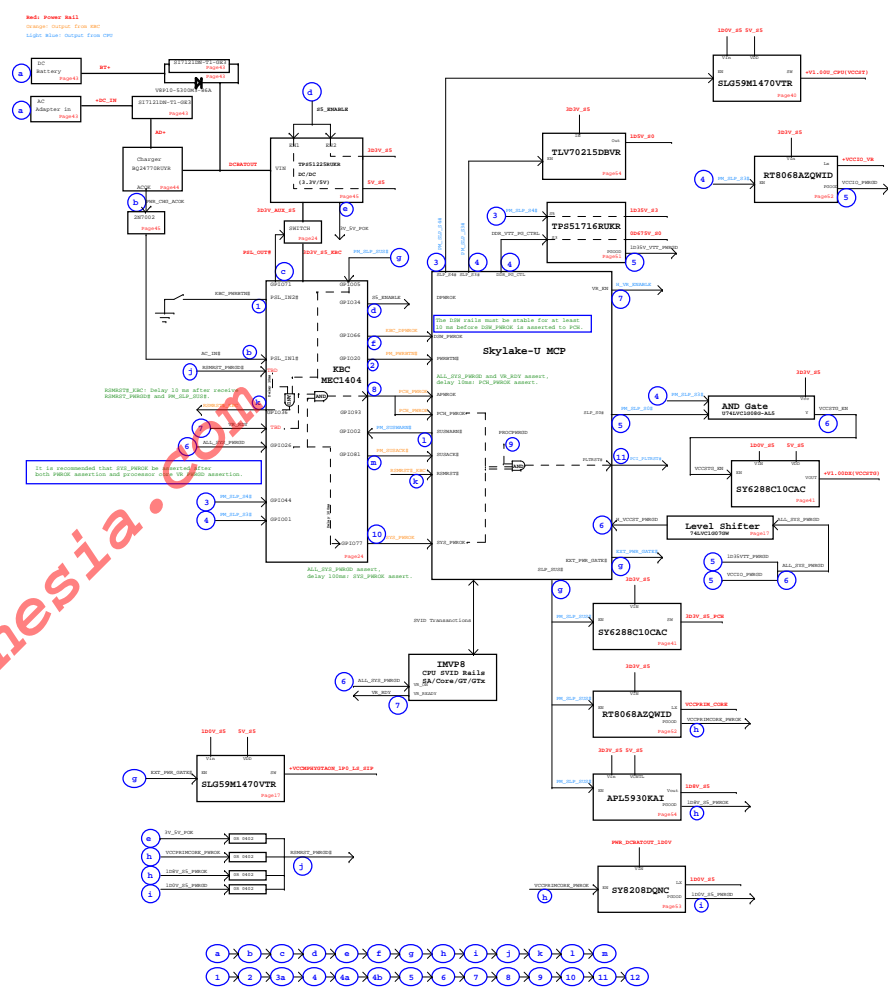
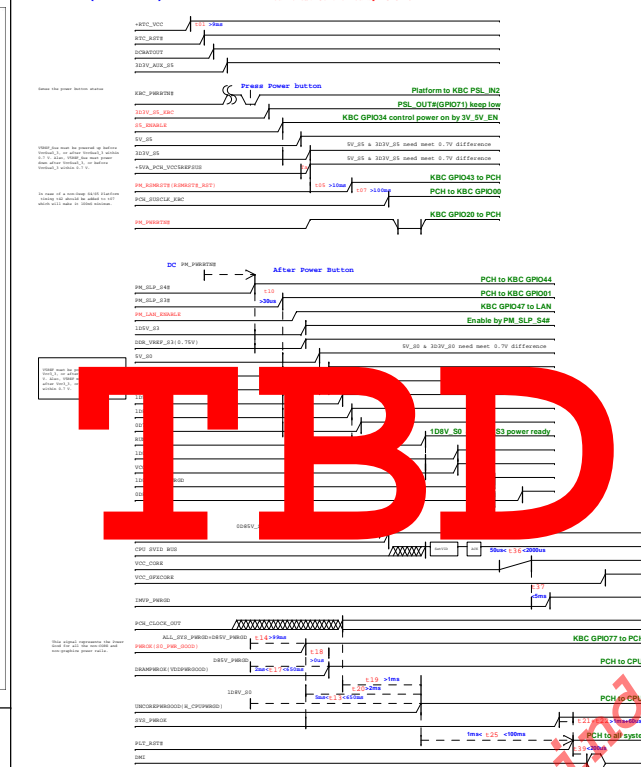
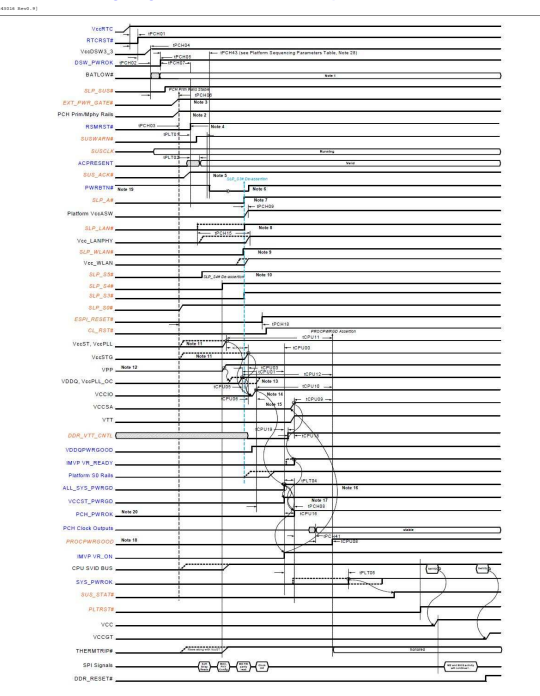


CLK Block Diagram



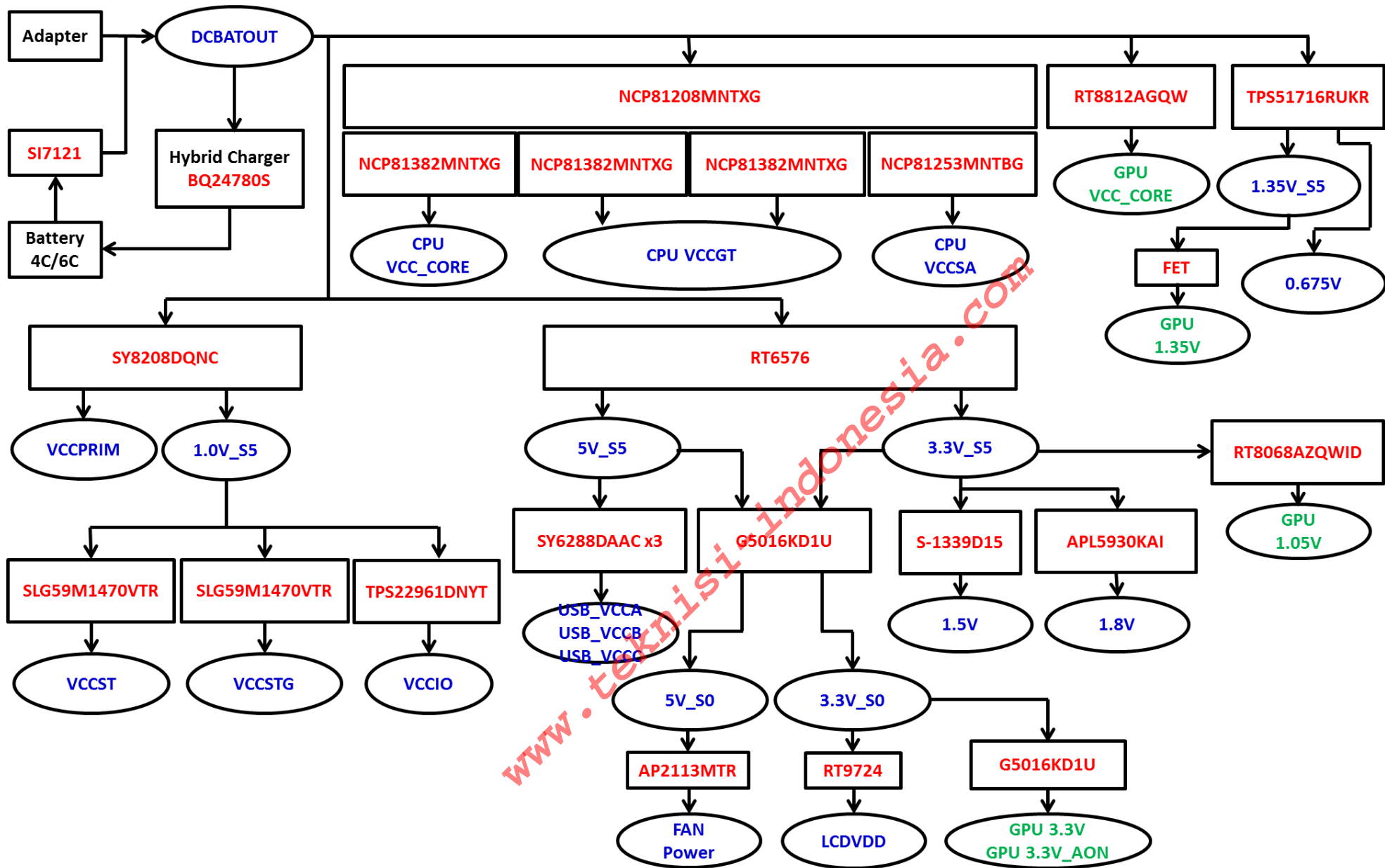
[illegible]

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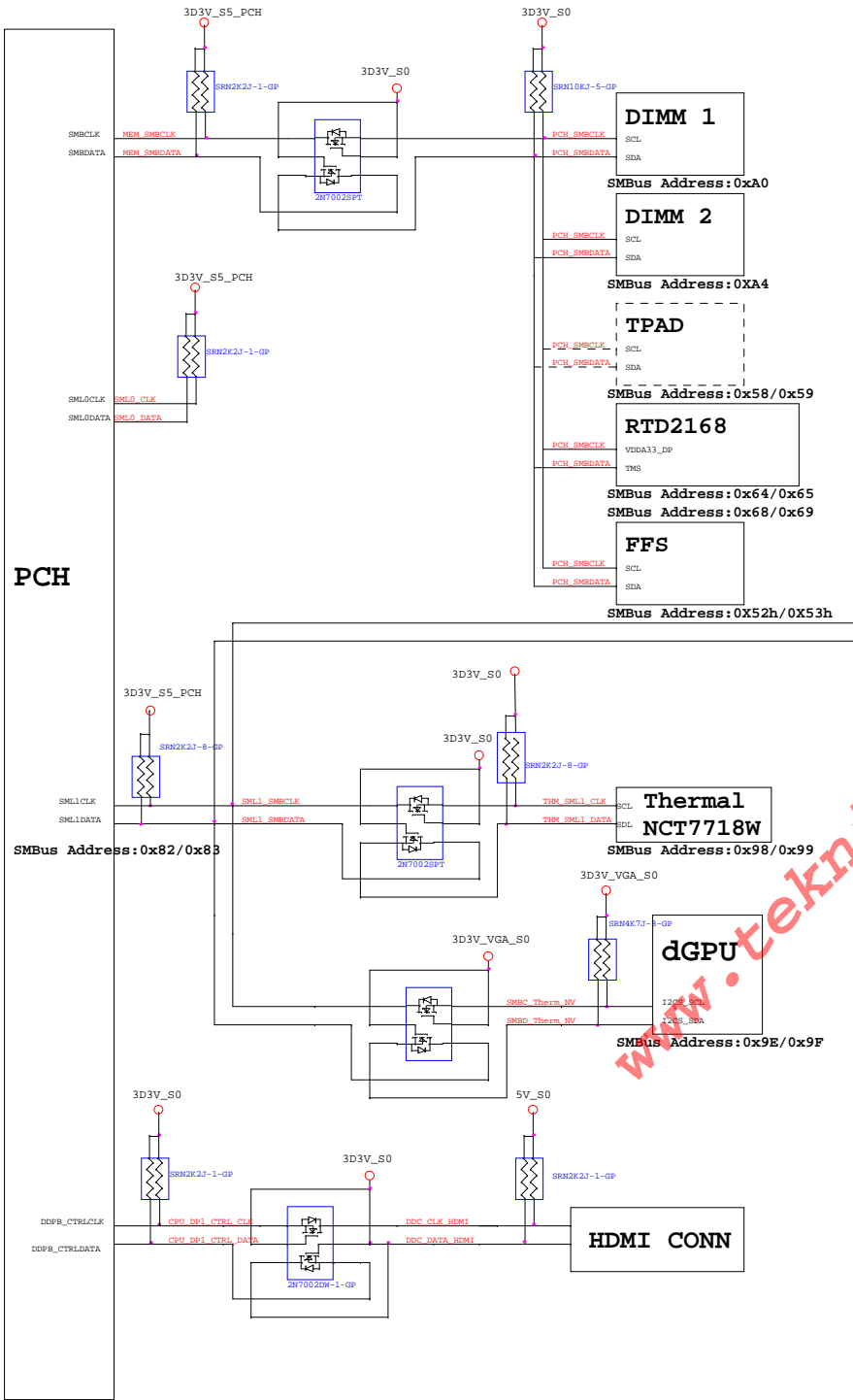


There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

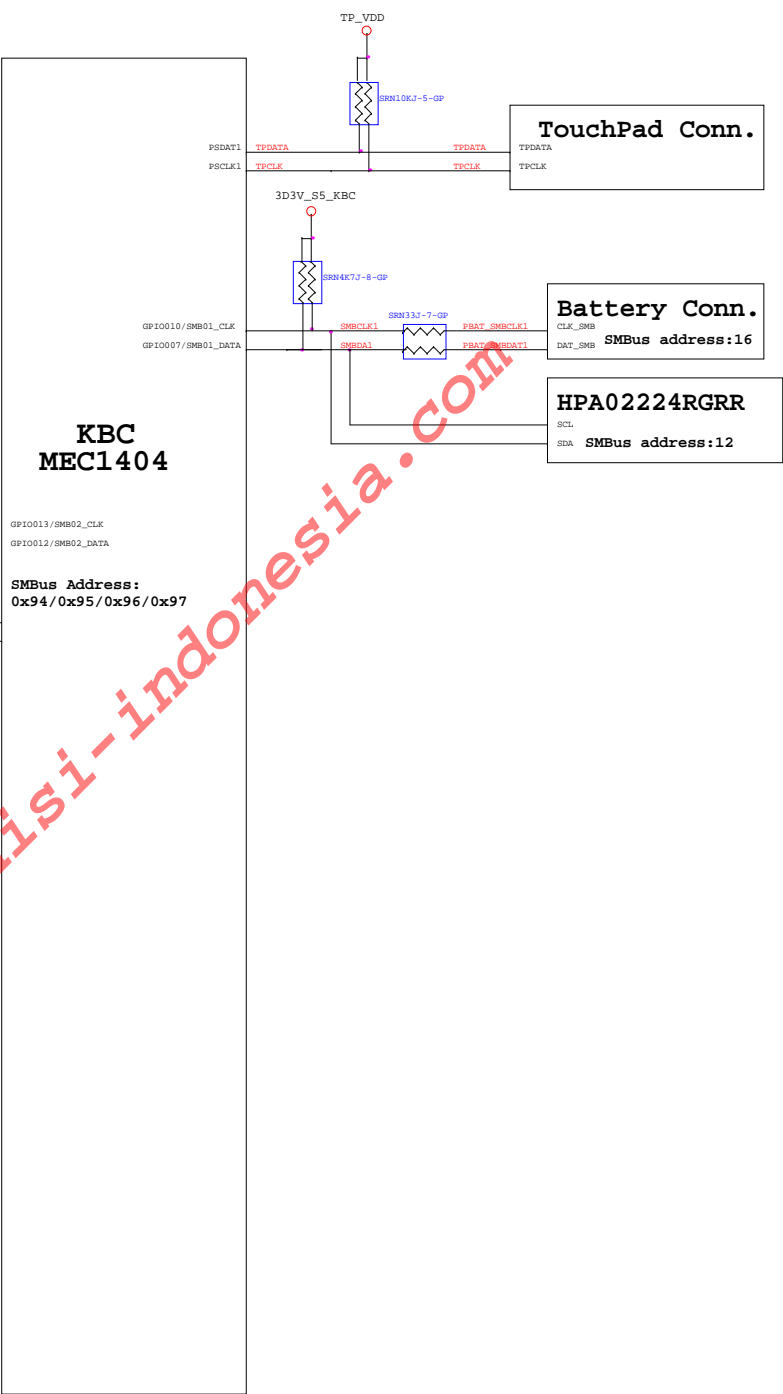
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During G6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q2 stays on.
- All delays should be minimized to increase time spent in G6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.



PCH SMBus Block Diagram



KBC SMBus Block Diagram





## Audio Block Diagram

